

RK61X

Technical Reference Manual

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Acronym Descriptions

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Chapter 1 Introduction

RK61X is a partner chip for Rockchip mobile application processor. It can minimize the external components in Rockchip's Table and TV BOX solution; reduce the total cost and PCB size.

RK61X includes two RGB display input interface with double data rate. With the internal MUX function, it can output 1080P HDMI signal to TV and output RGB/LVDS/MIPI signal to TFT panel. In this case, RK61X can support dual panel (TV and TFT) display.

RK61X includes an audio codec, which with two I2S/PCM interface, two differential microphone input and audio processing function.

RK61X provides a complete set of display interface to support very flexible applications as follows :

- 2 RGB display input interface with double data rate
- 1 LVDS display output interface with double channels
- 1 MIPI display output interface with 4 data lanes
- 1 HDMI display output interface
- 1 RGB display input interface shared with LVDS
- 1 RGB display input interface shared with RGB display input interface
- Audio interface: one 4ch I2S/PCM interface, one 1ch I2S/PCM interface and one SPDIF rx interface
- I2C configured interface

This document will provide guideline on how to use RK61X correctly and efficiently. The chapter 1 will introduce the features, block diagram, signal descriptions and system usage of RK61X, the chapter 2 to chapter 15 will describe the full function of each module in detail.

RK61X contains two versions: RK616 and RK618, the difference like follow: For RK616, it contains the chapters 2, 3, 4, 5, 8, 9, 10, 12, 13. For RK618, it contains the all chapters.

Table 1-1 The difference of RK616 and RK618

	RK616	RK618
PACKAGE	144-L	216-L
HDMI	support	support
SINGLE LVDS	support	support
DOUBLE LVDS	don't support	support
MIPI	don't support	support
ACODEC Normal	support	support
Charge Pump	don't support	support
VIF/SCALER	support	support

1.1 Features

1.1.1 Display interface

- Two 24BIT RGB input interface with dual data rate
- supports MIPI, LVDS and RGB interface to TFT LCD
- With scaler function, LVDS/MIPI/RGB and HDMI can output at the same time

1.1.2 HDMI

- Very low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 spec
- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
- Digital video interface supports a pixel size of 24bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug

1.1.3 LVDS

- 35MHz~150MHz clock support
- 28:4 data channel compression at data rates up to 945 Mbps per channel
- Support VGA, SVGA, XGA and single pixel SXGA
- Comply with the Standard TIA/EIA-644-A LVDS stand
- Support 8bit format-1, format-2, format-3 display mode, Support 6bit display mode.
- Display mode can be select by input MUX
- Low power mode

1.1.4 MIPI D-PHY

- Mixed-signal D-PHY mixed-signal hard-macro- LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™ MIPI® protocols
- 1.0GHz maximum data transfer rate per lane

- Expandable to support 4 data lanes, providing up to 4Gbps transfer rate
- HS, LP and ULPS modes supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: HS less than 3mA/Lane
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

1.1.5 MIPI Controller

- Support video and command modes
- PPI interface to the D-PHY
- Configurable from 1 to 4 data lanes output
- Supports up to 1Gb/s per data lane
- Bi-directional communication and escape mode support
- Programmable display resolutions, up to 2048x1080
- Multiple peripheral support capability with configurable virtual channels
- Video mode pixel formats: RGB565, RGB666 packed and loosely, RGB888
- Supports transmission of all generic commands
- ECC and checksum capabilities
- Supports ultra-low power mode
- Fault recovery schemes

1.1.6 Scaler

- Support max line pixel input upto 2560
- Support scaling down and scale up function
- Max output resolution 2048x1536

1.1.7 Audio Codec

- Two I2S/PCM interface
- Pure logic process, no need for Mixed signal process.
- Very low power, can be made <6.5mA in 3.3V for playback.
- 18 to 24 bit high order Sigma-Delta modulation for DAC with >93 dB SNR.
- 16 to 18 bit high order Sigma-Delta modulation for ADC with >90 dB SNR.
- Digital interpolation and decimation filter integrated.
- Line-in, microphone and speaker out interface.
- On-chip analog post filter and digital filters.
- Single-ended or differential microphone input.
- Automatic gain control for smooth audio recording.
- Sampling rate of 8k/12k/16k/24k/32k/48k/44.1k/96k Hz
- Support 16ohm to 32ohm headphone and speaker phone output.
- 3.3V analog +/-10% power supply for analog and 1.2/1.1/1.0V for digital core.
- Mono, Stereo supported.

1.1.8 Chip controll

- I2C slave interface
- External clock input for Chip working, this clock can share with MCLK (12M)
- Interrupt output for HDMI in and other function
- Two PLL , one for dual datarate input logic; the other for scaler

1.2 Block Diagram

The following diagram shows the basic block diagram for RK61X

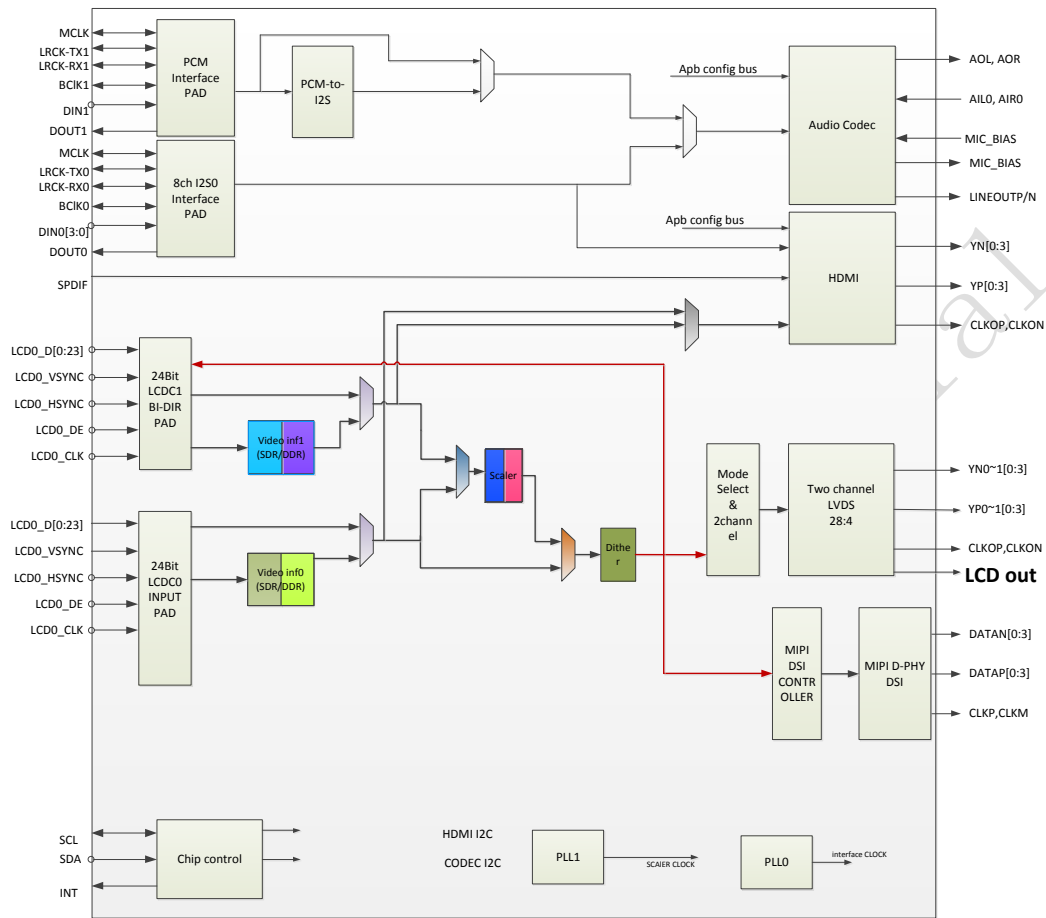


Fig. 1-1RK61X Block Diagram

1.3 Pin Description

In this chapter, the pin description is all power/ground descriptions in Table 1-1, include analog power/ground.

1.3.1 RK61X power/ground IO descriptions

Table 1-2 RK616 Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C3,C5,B7,C6,D5,F6,F7,G7,J11	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
	L10,E8,F9,C10,B12				

VCC	G5,J6	N/A	3.3	N/A	Digital IO Power
VDD	F5,F8,H7,D10	N/A	1.2	N/A	Internal Core Power
LVDS_VCC	A11,A12,B11, E10,F10	N/A	2.5	N/A	LVDS Analog power
PLL1VDD_1V2	J10	N/A	1.2	N/A	PLL1 1.2 power
PLL2VDD_1V2	K10	N/A	1.2	N/A	PLL2 1.2 power
PLL1VDD_3V3	K10	N/A	3.3	N/A	PLL1 3.3 power
PLL_VSS	K11	N/A	N/A	N/A	PLL analog ground
AVCC	C4,C7 A7,B8,B9	N/A	3.3	N/A	HDMI 3.3 analog power CODEC Analog power
HDMI_VDD	D6	N/A	1.2	N/A	HDMI 1.2 analog power

CODEC_AVSS	C8,D7	N/A	N/A	N/A	CODEC Analog ground
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Table 1-3 RK618 Power/Ground IO informations

Group	Ball #	Min(V)	Typ(V)	Max(V)	Descriptions
GND	C3,C8,C11,C14,F6,F7,F9 F11,G7,G8,G9,G10,H7,H8,H9 H10,J2,J6,J7,J8,J9,J10,K6,K7 K8,K9,K10,K11,L6,L9,L10,L11 P9,P12,R3	N/A	N/A	N/A	Internal Core Ground and Digital IO Ground
VCC	F8,G6,L7	N/A	3.3	N/A	Digital IO Power
VDD	H6,F10,L8	N/A	1.2	N/A	Internal Core Power
LVDS_VCC	P6,P8,P11	N/A	2.5	N/A	LVDS Analog power
PLL1VDD_1V2	L4	N/A	1.2	N/A	PLL1 1.2 power
PLL2VDD_1V2	L4	N/A	1.2	N/A	PLL2 1.2 power

PLL1VDD_3V3	L1	N/A	3.3	N/A	PLL1 3.3 power
PLL1VSS	K2	N/A	N/A	N/A	PLL analog ground
AVCC	R16,H16,K16,F16,D15,E15	N/A	3.3	N/A	HDMI 3.3 analog power CODEC Analog power
HDMIVDD	K15	N/A	1.2	N/A	HDMI 1.2 analog power
CODEC_AVSS	A7,B8,B9,E16,D16	N/A	N/A	N/A	CODEC Analog ground
HDMI_AVSS	L14,M14,P14,R15	N/A	N/A	N/A	HDMI Analog ground
MIPIPLL_3V3	M4	N/A	3.3	N/A	MIPI PLL analog power
MIPIAVDD_1V2	L3	N/A	1.2	N/A	MIPI analog power
MIPI_AVSS	L2,M3,P3,T3	N/A	N/A	N/A	MIPI analog ground

1.3.2 RK61X function IO descriptions

Table 1-4 RK61X IO descriptions

Port name	BALL# (144-L) RK616	BALL# (216-L) RK618	Pad dir	Reset value	Pull up/down	Power Supply	Pin Description
IO_LCDC1_DATA[8]	H8	E1	I/O	input	pull down	LCDC	LCD interface 1 data 8
IO_LCDC1_DATA[7]	G8	F5	I/O	input	pull down	LCDC	LCD interface 1 data 7
IO_LCDC1_DATA[6]	M9	F4	I/O	input	pull down	LCDC	LCD interface 1 data 6
IO_LCDC1_DATA[5]	L9	F3	I/O	input	pull down	LCDC	LCD interface 1 data 5
IO_LCDC1_DATA[4]	K9	F2	I/O	input	pull down	LCDC	LCD interface 1 data 4
IO_LCDC1_DATA[3]	J9	F1	I/O	input	pull down	LCDC	LCD interface 1 data 3
IO_LCDC1_DATA[2]	H9	G1	I/O	input	pull down	LCDC	LCD interface 1 data 2
IO_LCDC1_DATA[1]	G9	G2	I/O	input	pull down	LCDC	LCD interface 1 data 1
IO_LCDC1_DATA[0]	M10	H5	I/O	input	pull down	LCDC	LCD interface 1 data 0
IO_LCDC1_DEN	M11	H4	I/O	input	pull down	LCDC	lcdc1 data enable signal
IO_LCDC1_DCLKP	L11	H1	I/O	input	pull down	LCDC	lcdc1 clock out
IO_LCDC1_DCLKN	---	H2	I/O	input	pull down	LCDC	lcdc1 clock out(Negative)
IO_LCDC1_HSYNEN	M12	J1	I/O	input	pull down	LCDC	lcdc0 horizontal sync signal
IO_LCDC1_VSYNEN	L12	K1	I/O	input	pull down	LCDC	lcdc0 vertical sync signal
IO_I2S1SDO	H12	H3	O		pull down	LCDC	I2S1 SDO
IO_I2S1BCLK	J12	J5	I/O		pull down	LCDC	I2S1 SCLK
IO_I2S1SLRCKRX	K12	J4	I/O		pull down	LCDC	I2S1 LRCK for ADC
IO_I2S1SLRCKTX	H11	J3	I/O		pull down	LCDC	I2S1 LRCK for DAC
IO_I2S1SDI	G10	L5	I		pull down	LCDC	I2S1 SDI
IO_MIPIPHY_DATAN0	---	M1	A			MIPIPH Y	MIPI data lane0 serial data output(Negative)
IO_MIPIPHY_DATAPO	---	M2	A			MIPIPH Y	MIPI data lane0 serial data output
IO_MIPIPHY_DATAN1	---	N1	A			MIPIPH Y	MIPI data lane1 serial data output(Negative)
IO_MIPIPHY_DATAP1	---	N2	A			MIPIPH Y	MIPI data lane1 serial data output
IO_MIPIPHY_CLKN	---	P1	A			MIPIPH Y	MIPI clock lane serial data output(Negative)
IO_MIPIPHY_CLKP	---	P2	A			MIPIPH Y	MIPI clock lane serial data output
IO_MIPIPHY_DATAP2	---	R2	A			MIPIPH Y	MIPI data lane2 serial data output
IO_MIPIPHY_DATAN2	---	R1	A			MIPIPH Y	MIPI data lane2 serial data output(Negative)
IO_MIPIPHY_DATAP3	---	T2	A			MIPIPH Y	MIPI data lane3 serial data output
IO_MIPIPHY_DATAN3	---	T1	A			MIPIPH Y	MIPI data lane3 serial data output(Negative)
IO_LCDC_DEN	---	R4	O	0	pull down	RGB	lcdc data enable signal(LVDS used as RGB Output)
IO_LCDC_DCLK	---	T4	O	0	pull down	RGB	lcdc clock out
IO_LCDC_HSYNEN	---	N5	O	0	pull down	RGB	lcdc horizontal sync signal
IO_LCDC_VSYNEN	---	M6	O	0	pull down	RGB	lcdc0 vertical sync signal
IO_LCDC_DATA23	---	P5	O	0	pull down	RGB	LCD interface data 23

IO_LCDC_DATA22	---	N6	O	0	pull down	RGB	LCD interface data 22
IO_LCDC_DATA21	---	N8	O	0	pull down	RGB	LCD interface data 21
IO_LCDC_DATA20	---	M8	O	0	pull down	RGB	LCD interface data 20
IO_LVDS_PADN_8	---	T5	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_8	---	R5	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_CLKN2	---	T6	A			LVDS	Output clock (Negative)
IO_LVDS_CLKP2	---	R6	A			LVDS	Output clock
IO_LVDS_PADN_7	---	T7	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_7	---	R7	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_6	---	T8	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_6	---	R8	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_5	---	T9	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_5	---	R9	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_XRES	E9	T15	A			LVDS	LVDS current biasing generation
IO_LVDS_PADN_4	C11	T10	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADP_4	C12	R10	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_CLKN1	E11	T11	A			LVDS	Output clock (Negative)
IO_LVDS_CLKP1	E12	R11	A			LVDS	Output clock
IO_LVDS_PADN_3	D11	T12	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_3	D12	R12	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_2	F11	T13	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_2	F12	R13	A			LVDS	Transmit serial data out, n=1~8
IO_LVDS_PADN_1	G11	T14	A			LVDS	Transmit serial data out (Negative), n=1~8
IO_LVDS_PADP_1	G12	R14	A			LVDS	Transmit serial data out, n=1~8
IO_HDMI_EXTR	A2	T16	A			HDMI	Connect 1.9Kohm resistor to ground to generate reference current.
IO_HDMI_TX3N	A6	P15	A			HDMI	TMDS negative clock line
IO_HDMI_TX3P	B6	P16	A			HDMI	TMDS positive clock line.
IO_HDMI_TX0N	A5	N15	A			HDMI	TMDS channel 0 negative data line.
IO_HDMI_TX0P	B5	N16	A			HDMI	TMDS channel 0 positive data line.
IO_HDMI_TX1N	A4	M15	A			HDMI	TMDS channel 1 negative data line.
IO_HDMI_TX1P	B4	M16	A			HDMI	TMDS channel 1 positive data line.
IO_HDMI_TX2N	A3	L15	A			HDMI	TMDS channel 2 negative data line.
IO_HDMI_TX2P	B3	L16	A			HDMI	TMDS channel 2 positive data line.
IO_ACODEC_IN3L	B10	L13	A			ACODEC	Left line input

IO_ACODEC_IN3R	A10	M13	A			ACODEC	Right line input
IO_ACODEC_MIC1N	C9	J11	A			ACODEC	Negative input for left microphone
IO_ACODEC_MIC1P	---	J12	A			ACODEC	Positive input for left microphone
IO_ACODEC_MICBIAS1	D9	M11	A			ACODEC	Microphone bias output1
IO_ACODEC_MICBIAS2	---	L12	A			ACODEC	Microphone bias output2
IO_ACODEC_MIC2P	---	H13	A			ACODEC	Positive input for right microphone
IO_ACODEC_MIC2N	---	H12	A			ACODEC	Negative input for right microphone
IO_ACODEC_IN1N	---	F12	A			ACODEC	Negative line input
IO_ACODEC_IN1P	---	F13	A			ACODEC	Positive line input
IO_ACODEC_VCM	D8	J16	A			ACODEC	Common mode reference voltage decoupling pin
IO_ACODEC_LINE1	---	F14	A			ACODEC	Line output 1
IO_ACODEC_LINE2	---	H14	A			ACODEC	Line output 2
IO_ACODEC_SPKL	A8	J14	A			ACODEC	Left speaker output
IO_ACODEC_SPKR	A9	J15	A			ACODEC	Right speaker output
IO_ACODEC_HPL	---	F15	A			ACODEC	Left headphone output
IO_ACODEC_HPAGND_FB	---	G15	A			ACODEC	Floating, reserved for future
IO_ACODEC_HPR	---	G16	A			ACODEC	Right headphone output
IO_HDMI_CEC	E7	E13	I/O		pull up	LCDC	HDMI CEC control line.
IO_HDMI_HDP	E6	C16	I/O		pull up	LCDC	HDMI HPD Hot plug detect
IO_HDMI_I2CSDA	D4	N12	I/O		pull up	LCDC	DDC channel SDA in. For tri - state gate use
IO_HDMI_I2CSCL	E5	N11	I/O		pull up	LCDC	DDC channel SCL in. For tri - state gate use
IO_I2C_SDA	E2	M9	I/O		pull up	LCDC	I2C SDA
IO_I2C_SCL	D1	N9	I		pull up	LCDC	I2C SCL
IO_CLKIN	D2	C15	I		pull down	LCDC	RK61X clock input
IO_I2S0SDO	B2	E14	O		pull down	LCDC	I2S0 sdo
IO_I2S0BCLK	A1	B16	I/O		pull down	LCDC	I2S0 SCLK
IO_I2S0SLRCKRX	B1	B15	I/O		pull down	LCDC	I2S0 LRCK for ADC
IO_I2S0SLRCKTX	C2	A16	I/O		pull down	LCDC	I2S0 LRCK for DAC
IO_I2S0SDI[0]	C1	D12	I		pull down	LCDC	I2S0 sdi[0]
IO_I2S0SDI[1]	D3	E11	I		pull down	LCDC	I2S0 sdi[1]
IO_I2S0SDI[2]	E4	B14	I		pull down	LCDC	I2S0 sdi[2]
IO_I2S0SDI[3]	E3	A15	I		pull down	LCDC	I2S0 sdi[3]
IO_SPDIF	F4	H11	I		pull down	LCDC	SPDIF input
IO_TEST	F3	G11	I		pull down	LCDC	test input
IO_NPOR	F2	A14	I		pull up	LCDC	power on reset
IO_INT	E1	D11	I		pull down	LCDC	RK61X interrupt output
IO_LCDC0_VSYNEN	K5	B13	I		pull down	LCDC	lcdc0 vertical sync signal
IO_LCDC0_HSYNEN	L5	C12	I		pull down	LCDC	lcdc0 horizontal sync

							signal
IO_LCDC0_DEN	L4	A13	I		pull down	LCDC	lcdc0 data enable signal
IO_LCDC0_DCLKP	M5	A12	I		pull down	LCDC	lcdc0 clock out
IO_LCDC0_DCLKN	---	B12	I		pull down	LCDC	lcdc0 clock out(Negative)
IO_LCDC0_DATA[23]	F1	C9	I		pull down	LCDC	LCD interface 0 data 23
IO_LCDC0_DATA[22]	G1	B11	I		pull down	LCDC	LCD interface 0 data 22
IO_LCDC0_DATA[21]	G2	E9	I		pull down	LCDC	LCD interface 0 data 21
IO_LCDC0_DATA[20]	G3	A11	I		pull down	LCDC	LCD interface 0 data 20
IO_LCDC0_DATA[19]	G4	D9	I		pull down	LCDC	LCD interface 0 data 19
IO_LCDC0_DATA[18]	H1	B10	I		pull down	LCDC	LCD interface 0 data 18
IO_LCDC0_DATA[17]	H2	A10	I		pull down	LCDC	LCD interface 0 data 17
IO_LCDC0_DATA[16]	H3	B9	I		pull down	LCDC	LCD interface 0 data 16
IO_LCDC0_DATA[15]	H4	A9	I		pull down	LCDC	LCD interface 0 data 15
IO_LCDC0_DATA[14]	J1	A8	I		pull down	LCDC	LCD interface 0 data 14
IO_LCDC0_DATA[13]	J2	E8	I		pull down	LCDC	LCD interface 0 data 13
IO_LCDC0_DATA[12]	J3	B8	I		pull down	LCDC	LCD interface 0 data 12
IO_LCDC0_DATA[11]	J4	D8	I		pull down	LCDC	LCD interface 0 data 11
IO_LCDC0_DATA[10]	K1	A7	I		pull down	LCDC	LCD interface 0 data 10
IO_LCDC0_DATA[9]	K2	A6	I		pull down	LCDC	LCD interface 0 data 9
IO_LCDC0_DATA[8]	K3	B7	I		pull down	LCDC	LCD interface 0 data 8
IO_LCDC0_DATA[7]	K4	A5	I		pull down	LCDC	LCD interface 0 data 7
IO_LCDC0_DATA[6]	L1	B6	I		pull down	LCDC	LCD interface 0 data 6
IO_LCDC0_DATA[5]	L2	C6	I		pull down	LCDC	LCD interface 0 data 5
IO_LCDC0_DATA[4]	M1	A4	I		pull down	LCDC	LCD interface 0 data 4
IO_LCDC0_DATA[3]	M2	E6	I		pull down	LCDC	LCD interface 0 data 3
IO_LCDC0_DATA[2]	L3	B5	I		pull down	LCDC	LCD interface 0 data 2
IO_LCDC0_DATA[1]	M3	D6	I		pull down	LCDC	LCD interface 0 data 1
IO_LCDC0_DATA[0]	M4	D5	I		pull down	LCDC	LCD interface 0 data 0
IO_LCDC1_DATA[23]	J5	A3	I/O	input	pull down	LCDC	LCD interface 1 data 23
IO_LCDC1_DATA[22]	H5	A2	I/O	input	pull down	LCDC	LCD interface 1 data 22
IO_LCDC1_DATA[21]	M6	B4	I/O	input	pull down	LCDC	LCD interface 1 data 21
IO_LCDC1_DATA[20]	L6	A1	I/O	input	pull down	LCDC	LCD interface 1 data 20
IO_LCDC1_DATA[19]	K6	C5	I/O	input	pull down	LCDC	LCD interface 1 data 19
IO_LCDC1_DATA[18]	H6	B3	I/O	input	pull down	LCDC	LCD interface 1 data 18
IO_LCDC1_DATA[17]	G6	B2	I/O	input	pull down	LCDC	LCD interface 1 data 17
IO_LCDC1_DATA[16]	M7	B1	I/O	input	pull down	LCDC	LCD interface 1 data 16
IO_LCDC1_DATA[15]	L7	C1	I/O	input	pull down	LCDC	LCD interface 1 data 15
IO_LCDC1_DATA[14]	K7	C2	I/O	input	pull down	LCDC	LCD interface 1 data 14
IO_LCDC1_DATA[13]	J7	D1	I/O	input	pull down	LCDC	LCD interface 1 data 13
IO_LCDC1_DATA[12]	M8	E4	I/O	input	pull down	LCDC	LCD interface 1 data 12
IO_LCDC1_DATA[11]	L8	D2	I/O	input	pull down	LCDC	LCD interface 1 data 11
IO_LCDC1_DATA[10]	K8	E3	I/O	input	pull down	LCDC	LCD interface 1 data 10
IO_LCDC1_DATA[9]	J8	E2	I/O	input	pull down	LCDC	LCD interface 1 data 9

Notes :

①: Pad types : I = input , O = output , I/O = input/output (bidirectional) ,
AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value

- ③: Reset state: I = input without any pull resistor O = output
- ④: It is die location. For examples, "Left side" means that all the related IOs are always in left side of die
- ⑤: Power supply means that all the related IOs are in this IO power domain. If multiple powers are included, they are connected together in one IO power ring
- ⑥: The pull up/pull down is configurable.

1.4 Package information

1.4.1 RK616 Dimension

RK616 package is TFBGA (HF) 10x10 0.8P 144L_2L Substrate
(body: 10mm x 10mm ; ball size : 0.4mm ; ball pitch : 0.8mm)

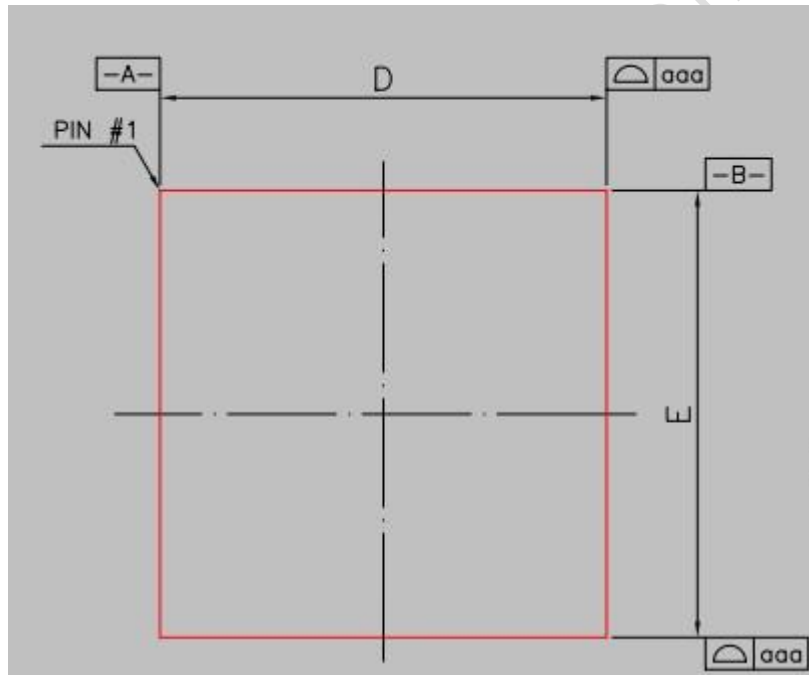


Fig. 1-2 RK616 TFBGA(HF) Package Top View

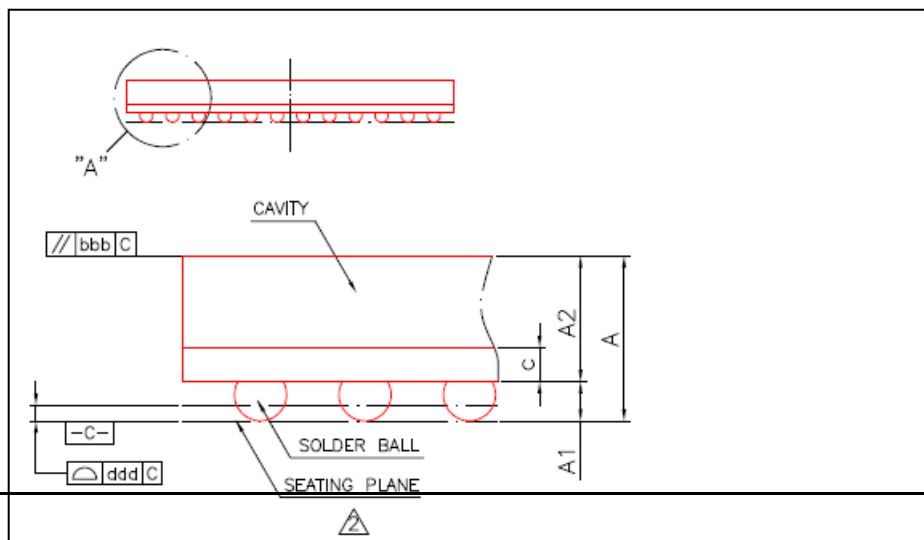


Fig. 1-3 RK616 TFBGA(HF) Package Side View

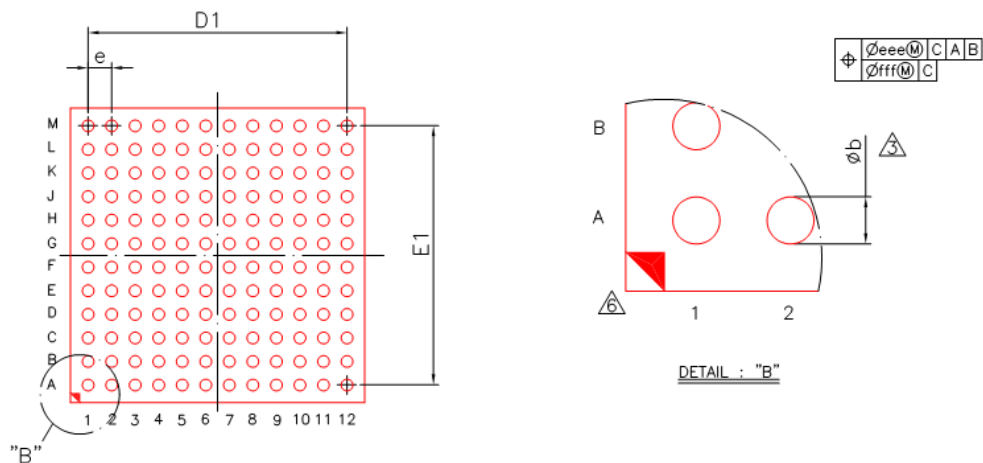


Fig. 1-4 RK616 TFBGA(HF) Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	8.80	---	---	0.346	---
E1	---	8.80	---	---	0.346	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	12/12			12/12		

Fig. 1-5 RK616 TFBGA(HF) Package Dimension

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RK618 package is TFBGA (HF) 11x11 0.65P 216L_2L Substrate
(body: 11mm x 11mm ; ball size : 0.3mm ; ball pitch : 0.65mm)

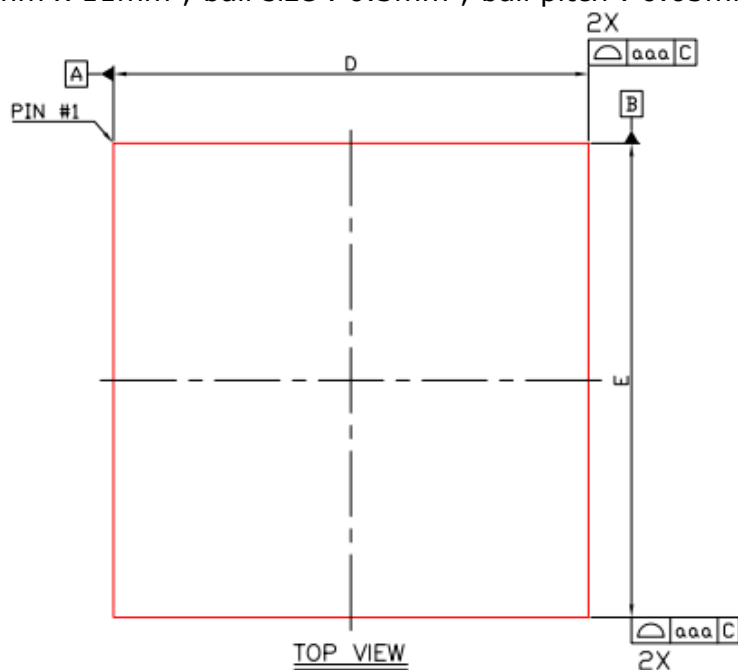


Fig. 1-6 RK618 TFBGA(HF) Package Top View

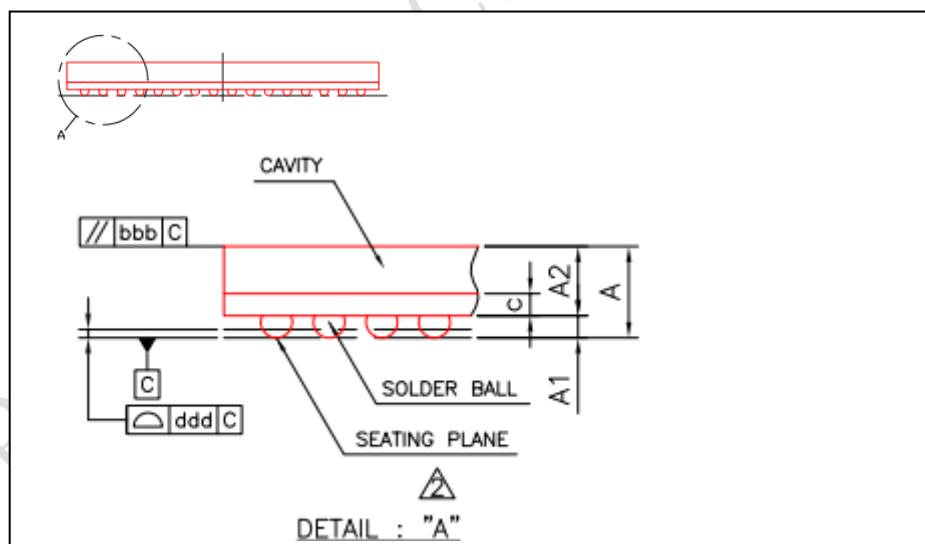


Fig. 1-7 RK618 TFBGA(HF) Package Side View

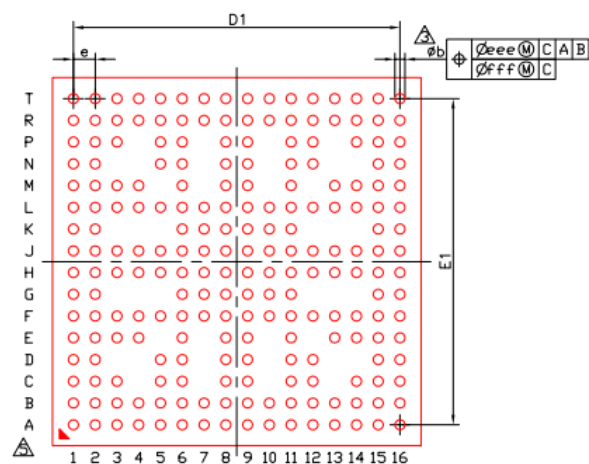


Fig. 1-8 RK618 TFBGA(HF) Package Bottom View

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.91	0.96	1.01	0.036	0.038	0.040
c	0.22	0.26	0.30	0.009	0.010	0.012
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	----	9.75	----	----	0.384	----
E1	----	9.75	----	----	0.384	----
e	----	0.65	----	----	0.026	----
b	0.25	0.30	0.35	0.010	0.012	0.014
aaa	0.15			0.006		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	16 /16			16 /16		

Fig. 1-9 RK618 TFBGA(HF) Package Dimension

1.4.3 RK616 Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	
A	I2S0_SCLK	HDMI_EXTR	HDMI_TX2N	HDMI_TX1N	HDMI_TX0N	HDMI_TXCN	CODEC_AVC_C	AOL	AOR	IN3R	LVDS_VCC	LVDS_VCC	A
B	I2S0_LRCK_RX	I2S0_SDO	HDMI_TX2P	HDMI_TX1P	HDMI_TX0P	HDMI_TXCP	VSS	CODEC_AVC_C	CODEC_AVC_C	IN3L	LVDS_VCC	VSS	B
C	I2S0_SDI_D0	I2S0_LRCK_TX	VSS	HDMI_VCC_3V3	VSS	VSS	HDMI_VCC_3V3	CODEC_AVS_S	MIC1N	VSS	LCD_D9/LVD_S0_D3N	LCD_D8/LVD_S0_D3P	C
D	I2C_SCL	I2C_CLK	I2S0_SDI_D1	HDMI_SDA	VSS	HDMI_VDD_1V2	CODEC_AVS_S	VCM	MICBIAS1	VDD	LCD_D5/LVD_S0_D2N	LCD_D4/LVD_S0_D2P	D
E	INT	I2C_SDA	I2S0_SDI_D3	I2S0_SDI_D2	HDMI_SCL	HDMI_HPD	HDMI_CEC	VSS	LVDS_EXTR	LVDS_VCC	LCD_D7/LVD_S0_CLKN	LCD_D6/LVD_S0_CLKP	E
F	LCD0_D23	NPOR	TEST	SPDIF	VDD	VSS	VSS	VDD	VSS	LVDS_VCC	LCD_D3/LVD_S0_D1N	LCD_D2/LVD_S0_D1P	F
G	LCD0_D22	LCD0_D21	LCD0_D20	LCD0_D19	VCC	LCD1_D17	VSS	LCD1_D7	LCD1_D1	I2S1_SDI	LCD_D1/LVD_S0_D0N	LCD_D0/LVD_S0_D0P	G
H	LCD0_D18	LCD0_D17	LCD0_D16	LCD0_D15	LCD1_D22	LCD1_D18	VDD	LCD1_D8	LCD1_D2	PLL1VDD_3V3	I2S1_LRCK_TX	I2S1_SDO	H
J	LCD0_D14	LCD0_D13	LCD0_D12	LCD0_D11	LCD1_D23	VCC	LCD1_D13	LCD1_D9	LCD1_D3	PLL1VDD_1V2	VSS	I2S1_SCLK	J
K	LCD0_D10	LCD0_D9	LCD0_D8	LCD0_D7	LCD0_VSYNC	LCD1_D19	LCD1_D14	LCD1_D10	LCD1_D4	PLL2VDD_1V2	PLL_VSS	I2S1_LRCK_RX	K
L	LCD0_D8	LCD0_D5	LCD0_D2	LCD0_DEN	LCD0_HSYNC	LCD1_D20	LCD1_D15	LCD1_D11	LCD1_D5	VSS	LCD1_DCLK	LCD1_VSYNC	L
M	LCD0_D4	LCD0_D3	LCD0_D1	LCD0_D0	LCD0_DCLK	LCD1_D21	LCD1_D16	LCD1_D12	LCD1_D6	LCD1_D0	LCD1_DEN	LCD1_HSYNC	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Fig. 1-10 RK616 Ball Mapping Diagram

1.4.4 RK618 Ball Map

216	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		
A	LCD1_D20	LCD1_D22	LCD1_D23	LCD0_D4	LCD0_D7	LCD0_D9	LCD0_D10	LCD0_D14	LCD0_D15	LCD0_D17	LCD0_D20	LCD0_DCLKP	LCD0_DEN	NPOR	I2S0_SDI_D3	I2S0_LRCK_TX	A	
B	LCD1_D16	LCD1_D17	LCD1_D18	LCD1_D21	LCD0_D2	LCD0_D6	LCD0_D8	LCD0_D12	LCD0_D16	LCD0_D18	LCD0_D22	LCD0_DCLKN	LCD0_VSYNC	I2S0_SDI_D2	I2S0_LRCK_RX	I2S0_SCLK	B	
C	LCD1_D15	LCD1_D14	VSS		LCD1_D19	LCD0_D5		VSS	LCD0_D23		VSS	LCD0_HSYNC		VSS	I2S0_CLK	HDMI_HPD	C	
D	LCD1_D13	LCD1_D11			LCD0_D0	LCD0_D1		LCD0_D11	LCD0_D19		INT	I2S0_SDI_D0			CODEC_A_VCC1	CODEC_A_VSS	D	
E	LCD1_D8	LCD1_D9	LCD1_D10	LCD1_D12		LCD0_D3		LCD0_D13	LCD0_D21		I2S0_SDI_D1		HDMI_CEC	I2S0_SDO	CODEC_A_VCC1	CODEC_A_VSS	E	
F	LCD1_D3	LCD1_D4	LCD1_D5	LCD1_D6	LCD1_D7	VSS	VSS	LCD0_VCC0	VSS	VDD	VSS	IN1N	IN1P	LINE1	HPL	CODEC_A_VCC1	F	
G	LCD1_D2	LCD1_D1				LCD0_VCC1	VSS	VSS	VSS	VSS	TEST				HPAGNDP	HPR	G	
H	LCD1_DCLKP	LCD1_DCLKN	I2S1_SDO	LCD1_DEN	LCD1_D0	VDD	VSS	VSS	VSS	VSS	SPDIF	MIC2N	MIC2P	LINE2		CODEC_A_VSS	CODEC_A_VCC1	H
J	LCD1_HSYNC	VSS	I2S1_LRCK_TX	I2S1_LRCK_RX	I2S1_SCLK	VSS	VSS	VSS	VSS	VSS	MIC1N	MIC1P	CODEC_A_VSS	AOL	AOR	VCM	J	
K	LCD1_VSYNC	PLL_VSS				VSS	VSS	VSS	VSS	VSS	VSS				HDMI_VDD_1V2	CODEC_A_VCC2	K	
L	PLL_VDD_3V3	MIP1_AVSS	MIP1VDD_1V2	PLL_VDD_1V2	I2S1_SDI	VSS	LCD0_VCC2	VDD	VSS	VSS	VSS	MICBIAS2	IN3L	HDMI_AVS_S	HDMI_TX2_N	HDMI_TX2_P	L	
M	MIP1_D0N	MIP1_D0P	MIP1_AVSS	MIP1PLL_V2		LCD0_HSYNC		LCD0_D20	I2C_SDA		MICBIAS1		IN3N	HDMI_AVS_S	HDMI_TX1_N	HDMI_TX1_P	M	
N	MIP1_D1N	MIP1_D1P			LCD0_VSYNC	LCD0_D22		LCD0_D21	I2C_SCL		HDMI_SCL	HDMI_SDA			HDMI_TX0_N	HDMI_TX0_P	N	
P	MIP1_CLKN	MIP1_CLKP	MIP1_AVSS		LCD0_D23	LVDS_VCC		LVDS_VCC	VSS		LVDS_VCC	VSS			HDMI_AVS_S	HDMI_TX0_N	HDMI_TX0_P	P
R	MIP1_D2N	MIP1_D2P	VSS	LCD0_DEN	LCD0_D16/VDS1_D3P	LCD0_D14/VDS1_D3P	LCD0_D12/VDS1_D1P	LCD0_D10/VDS1_D0N	LCD0_D8/VDS1_D3P	LCD0_D6/VDS1_D3P	LCD0_D4/VDS1_D3P	LCD0_D2/VDS1_D3P	LCD0_D0/VDS1_D3P		HDMI_AVS_S	CODEC_A_VCC1	R	
T	MIP1_D3N	MIP1_D3P	MIP1_AVSS	LCD0_DCLK	LCD0_D18/VDS1_D3N	LCD0_D17/VDS1_CLKN	LCD0_D15/VDS1_D3N	LCD0_D13/VDS1_D1N	LCD0_D11/VDS1_D0N	LCD0_D9/VDS1_D3N	LCD0_D7/VDS1_CLKN	LCD0_D5/VDS1_D3N	LCD0_D3/VDS1_D1N	LCD0_D1/VDS1_D0N	LVDS_EXT_R	HDMI_EXT_R	T	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		

Fig. 1-11 RK618 Ball Mapping Diagram

1.5 Electrical Specification

1.5.1 Electrical Characteristics for General IO

Table1-5RK61X Electrical DC Characteristics for Digital General IO

Parameters		Symbol	Min	Typ	Max
Digital GPIO @3.3V	Pre-driver supply voltage	VDD	1.08V	1.2V	1.32V
	I/O supply voltage	VCC	2.97V	3.3V	3.63V
	Input High Voltage	VIH	2.0V	N/A	VCC+
	Input Low Voltage	VIL	-0.3V	N/A	0.8V
	Threshold point	VT	1.21V	1.42V	1.64V
	Schmitt trig Low to High threshold point	VT+	1.36V	1.60V	1.86V
	Schmitt trig. High to Low threshold point	VT-	0.93V	1.09V	1.30V
	Junction Temperature	TJ	0℃	25℃	125℃
	Input Leakage Current	IL			±1uA
	Tri-State output leakage current	IOZ			±1uA
	Pull-up Resistor	RPU	33K	41K	62K
	Pull-down Resistor	RPD	33K	42K	68K
	Output low voltage @IOL=2,4...24mA	VOL			0.4V
	Output high voltage @ IOH=2,4...24mA	VOH	2.4V		
	Low level output current @VOL=0.4V	IOL	8.0mA	12.4mA	15.6mA
	High level output current @VOH=2.4V	IOH	9.2mA	19.6mA	30.8mA

Table1-6RK61X Electrical AC Characteristics for Digital General IO

Type	Condition
Digital GPIO @3.3V	Typical case VCC=3.3V, VDD=1.2V temperature=25℃ Process = Typical-Typical
	Best case VCC=3.63V, VDD=1.32V temperature=0℃ Process = Fast-Fast
	Worst case VCC=2.97V, VDD=1.08V temperature=125℃ Process =Slow-Slow
	Worst case (low temperature) VCC=2.97V, VDD=1.08V temperature=-40℃ Process =Slow-Slow
	Best case (Low temperature) VCC=3.63V, VDD=1.32V temperature=-40℃ Process = Fast-Fast
	Best case (High) VCC=3.63V, VDD=1.32V temperature=125℃ Process = Fast-Fast

temperature)

1.6 Hardware Guideline

1.6.1 HDMI PCB Layout Guide

This section describes the strategy of PCB layout for customer integration with HDMI Transmitter on their PCB system. It mainly introduces how to connect the TMDS channel, DDC channel, CEC channel and HPD signal of Innosilicon HDMI Transmitter to the HDMI port type A.

Designers should include decoupling and bypass capacitors at each power pin in the layout. Place these components as closely as possible to the power pins.

The differential lines should be routed as directly as possible from chip to connector. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. The distance separating the two traces of the differential pair should be kept to a minimum. Layout all the differential pairs (+/-) with controlled impedance of 100 ohm differential. It is important that the differential lines be referenced to a solid plane.

1, TMDS CHANNEL

As the PCB scheme shown below

Connect TX3N to CK- on the HDMI PORT.

Connect TX3P to CK+ on the HDMI PORT.

Connect TX0N to TM0- on the HDMI PORT.

Connect TX0P to TM0+ on the HDMI PORT.

Connect TX1N to TM1- on the HDMI PORT.

Connect TX1P to TM1+ on the HDMI PORT.

Connect TX2N to TM2- on the HDMI PORT.

Connect TX2P to TM2+ on the HDMI PORT.

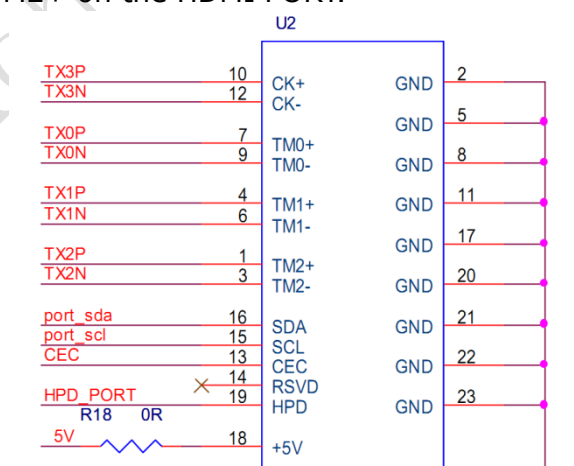


Fig. 1-12 PCB Scheme for TMDS Channel

2, DDC CHANNEL

The DDC channel used the industrial standard I2C bus. As shown the PCB

Scheme below, the DDC_sda and DDC_scl on the HDMI TX must be changed the working voltage from 3.3V to 5V by the component UPA672T. The DDC_sda and DDC_scl on HDMI TX side must be pulled up through a 10K resistor to 3.3V DC power. The port_sda and port_scl on the HDMI port side must be pulled up through a 10K resistor to 5V DC power.

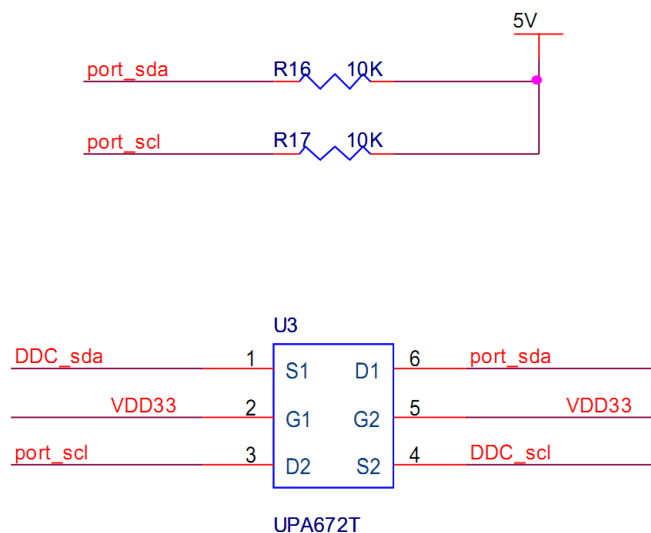


Fig. 1-13PCB Scheme for DDC Channel

3,CEC CHANNEL

The signal CEC_sda on the HDMI Transmitter must be pulled up through a 10K resistor to 3.3V DC power, then directly connect to CEC pad on the HDMI port.

4,HPD

As shown the PCB scheme below, it gives the reference circuit for customer connecting HPD signal of the HDMI Transmitter to the HPD_PORT pad on the HDMI port.

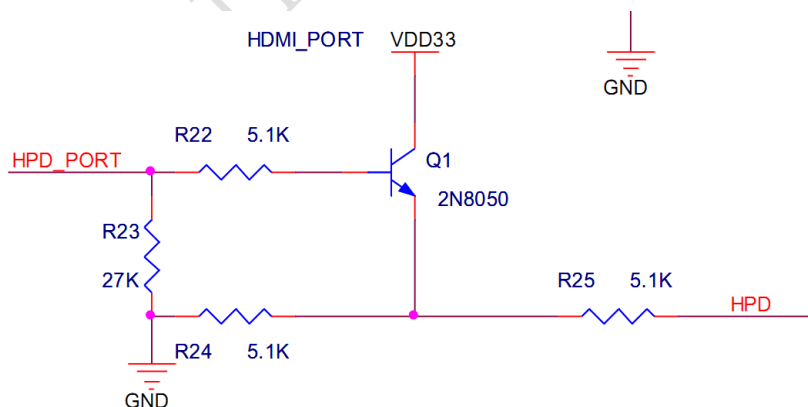


Fig. 1-14PCB Scheme for hpd

5,ESD

If ESD suppression devices or common mode chokes are used, place them near the HDMI connector.

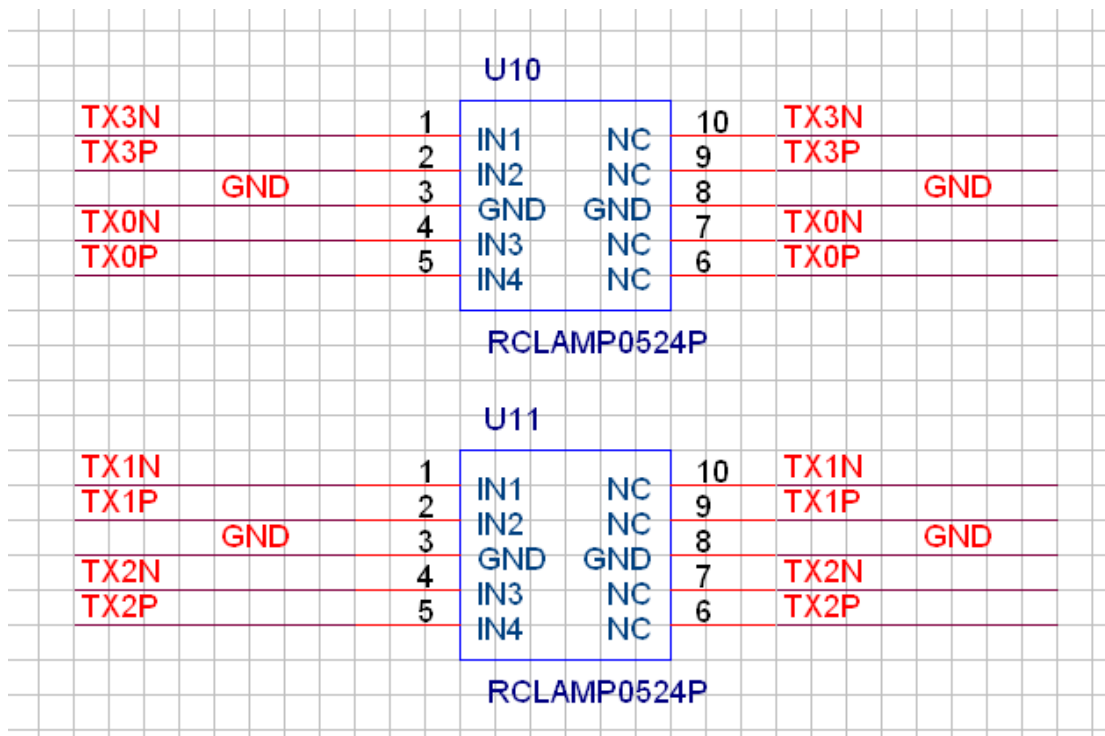


Fig. 1-15PCB Scheme for ESD

1.6.2 CODEC PCB Layout Guide

This chapter describes the strategy of PCB layout for customer integration with Codec in their PCB system. It mainly introduces how to connect the Codec signals.

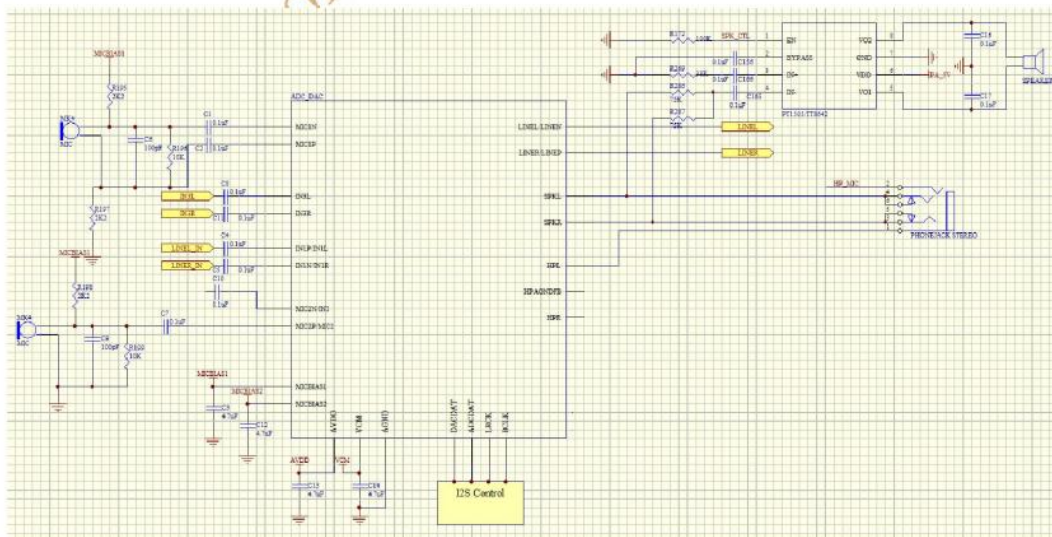


Fig. 1-16PCB Scheme for CODEC

Look at above diagram the MIC1N and MIC1P are each connected with a MIC through a 0.1uF CAP.

The C1 are formed a filter for the MIC, and the C7 have same function.

The MICBIAS is used for bias the MIC through a resistor. The resistor value should be changed according the MIC.

The AVDD should be supplied by 3V. The CAP connected with AVDD should be placed as close as possible

The VCM is connected with GND through a 4.7uF CAP. The CAP should be placed as close as possible.

The CPVDD should be supplied by 1.8V. The CAP connected with AVDD should be placed as close as possible

CPVDD,CPVEE,CBP,CBN,CPGND are formed a chargpump, then the DC level of the HPL and HPR would become zero, also the 100uF CAP could be canceled between the earphone and IC.

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Chapter 2 I2C

2.1 Overview

The I2C module controls all registers in jettaplus.

2.1.1 Features

External clock input for Chip working, this clock is 12MHz

Support I2C bus to APB bus convert

2.2 Block Diagram

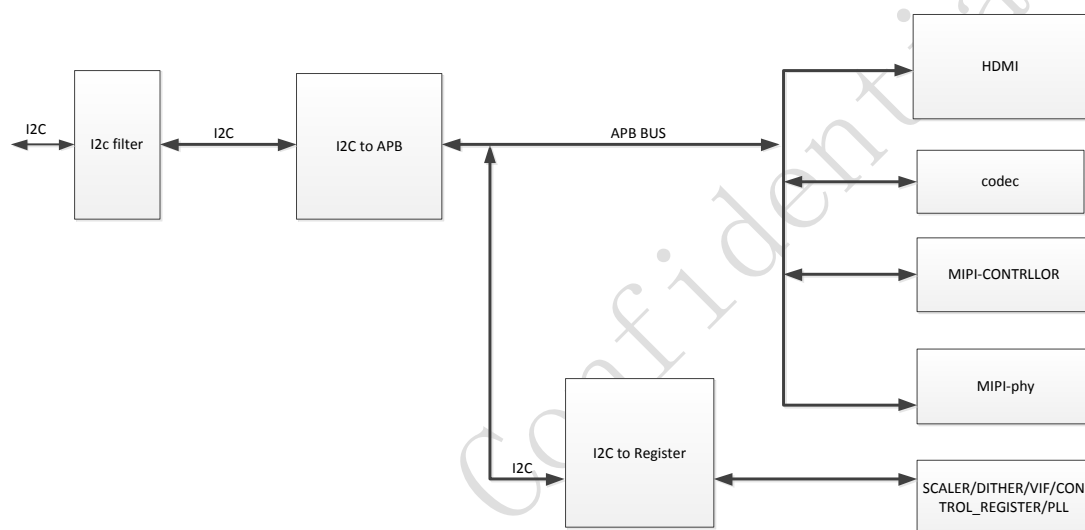


Fig. 2-1 I2C Block Diagram

I2C glitch filer module is used to filter glitch on I2C_SDA/I2C_SCL line.

I2C to APB block is used to control all blocks of jettaplus. For scaler/dither/vif/pll, they are I2C interface, we configure them directly through I2C bus. For HDMI/CODEC/MIPI-CONTROLLER/MIPI-PHY, they are APB interface, we configure them through I2C to APB module.

2.3 Function Description

2.3.1 I2C Write/Read operation

1. I2C Writing



Fig. 2-2 I2C Writing Operation

2. I2C Reading



Fig. 2-3 I2C Reading Operation

For jettaplus i2c slave, it expand the 7-bit addressing mode.

For I2C writing operation, please see Fig. 22-2. I2C master works in tx only mode. First transmit DEVICE ADDR, then begin to transmit 2byte REGISTER ADDR, low 8-bit first transmit. And then transmit 4byte data, low 8-bit first

transmit, the most 8-bit last transmit, then finish transaction. I2C slave receive each byte must return one ACK to I2C master.

For I2C reading operation, please see Fig.22-3. I2C master works in mix mode. First transmit 2byte REGISTER ADDR, write them into I2C module. Then restart(Sr), then transmit 1byte DEVICE ADDR, and then read data from I2C slave, first receive low 8-bit, last receive the most 8-bit.

3. Register Address Assignment

The jettaplus has only one device address, it is 0x50,all module use this device address.

The register address is shown as below:

Table2-1jettaplus register address assignment

Module	Register Address
scaler/dither/vif/pll	0x0000~0x03ff
HDMI	0x0400~0x07ff
CODEC	0x0800~0x0bff
MIPI-PHY	0x0C00~0x0fff
MIPI-CTRL	0x1000~0x13ff

2.3.2 I2C glitch filter

I2C glitch filter is designed for avoiding the I2C communication error because of SDA and SCL signal glitches.

The SCL and SDA input signals from I2C bus are filtered(both positive edge and negative edge) by the glitch filter block, then they are input to the three I2C TO APB module. The glitch filter timeout values of both positive edge and negative edge can setting in the through I2C interface.

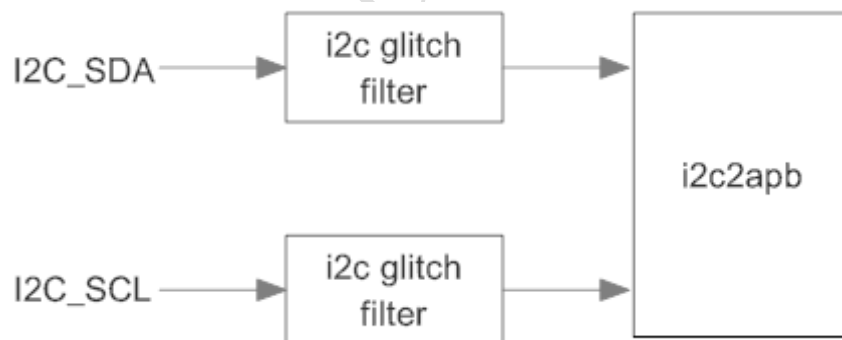


Fig. 2-4 I2C Glitch Filter

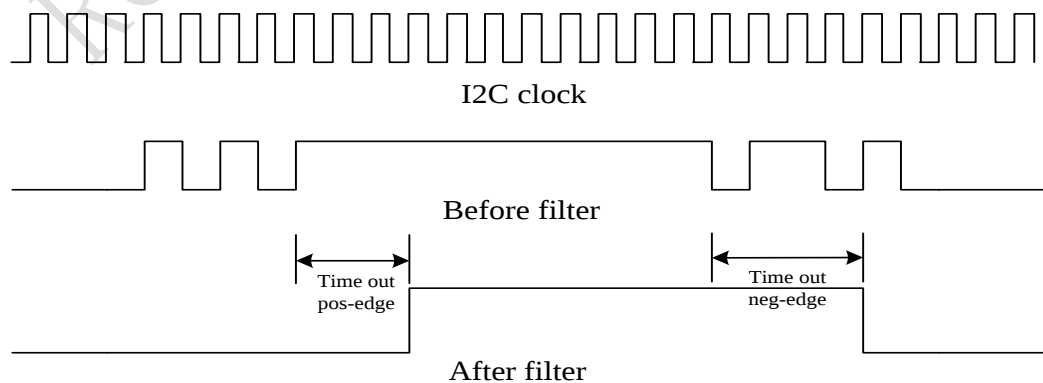


Fig.2-4I2C Glitch Filter Waveform

2.4 Register Description

2.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
VIF_VIF0_REG_0	0x0000	W	0x00000000	vif0 ctrl register
VIF_VIF0_REG_1	0x0004	W	0x00000000	vif0 setting register
VIF_VIF0_REG_2	0x0008	W	0x00000000	vif0 horizontal timing setting
VIF_VIF0_REG_3	0x000c	W	0x00000000	horizontal timing active
VIF_VIF0_REG_4	0x0010	W	0x00000000	vertical timing
VIF_VIF0_REG_5	0x0014	W	0x00000000	vertical timing active
VIF_VIF1_REG_0	0x0018	W	0x00000000	vif1 ctrl register
VIF_VIF1_REG_1	0x001c	W	0x00000000	vif1 setting register
VIF_VIF1_REG_2	0x0020	W	0x00000000	vif1 horizontal timing setting
VIF_VIF1_REG_3	0x0024	W	0x00000000	horizontal timing active
VIF_VIF1_REG_4	0x0028	W	0x00000000	vertical timing
VIF_VIF1_REG_5	0x002c	W	0x00000000	vertical timing active
Scaler_SCL_REG_0	0x0030	W	0x00000000	scaler ctrl register
Scaler_SCL_REG_1	0x0034	W	0x00000000	scaler horizontal/vertical factor register
Scaler_SCL_REG_2	0x0038	W	0x00000000	scaler output scanning start setting register
Scaler_SCL_REG_3	0x003c	W	0x00000000	scaler output scanning horizontal timing
Scaler_SCL_REG_4	0x0040	W	0x00000000	scaler output horizontal active window
Scaler_SCL_REG_5	0x0044	W	0x00000000	scaler output scanning vertical timing
Scaler_SCL_REG_6	0x0048	W	0x00000000	scaler output vertical active window
Scaler_SCL_REG_7	0x004c	W	0x00000000	scaler output horizontal border window
Scaler_SCL_REG_8	0x0050	W	0x00000000	scaler output vertical border window
FRC_REG_0	0x0054	W	0x00000000	dither frc control
CRU_CRU_CLKSEL0_CON	0x0058	W	0x00000000	Internal clock select and divide register
CRU_CRU_CLKSEL1_CON	0x005c	W	0x00000000	acodec/scaler clk cfg
CRU_CRU_CLKSEL2_CON	0x0060	W	0x00000000	acodec frac div
CRU_CRU_CLKSEL3_CON	0x0064	W	0x00000000	vif0/vif1/hdmi/mipi clock cfg
CRU_CRU_PLL0_CON0	0x0068	W	0x00000000	PLL0 control register0
CRU_CRU_PLL0_CON1	0x006c	W	0x00000000	PLL0 control register1
CRU_CRU_PLL0_CON2	0x0070	W	0x00000000	PLL0 control register1
CRU_CRU_PLL1_CON0	0x0074	W	0x00000000	PLL1 control register0
CRU_CRU_PLL1_CON1	0x0078	W	0x00000000	PLL1 control register1
CRU_CRU_PLL1_CON2	0x007c	W	0x00000000	PLL1 control register1
CRU_I2C_CON0	0x0080	W	0x00000000	i2c filter cfg register
CRU_LVDS_CON0	0x0084	W	0x00000020	Lvds config register
CRU_IO_CON0	0x0088	W	0x00000000	IO CFG register pull-up/pull-down/output enable

Name	Offset	Size	Reset Value	Description
CRU_IO_CON1	0x008c	W	0x00000000	IO CFG register schmitt input enable
CRU_pcm2is2_con0	0x0090	W	0x00000000	pcm2is2con0
CRU_pcm2is2_con1	0x0094	W	0x00000000	pcm2is2con1
CRU_pcm2is2_con2	0x0098	W	0x00000000	pcm2is2_con2
CRU_cfg_misc_con	0x009c	W	0x00000000	Misc register

Notes: Size: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

2.4.2 Detail Register Description

VIF_VIF0_REG_0

Address: Operational Base + offset (0x0000)

vif0 ctrl register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3	RW	0x0	vif0_diffclk_en Video Interface DDR clock mode 1'b0: single clock 1'b1: differential clocks
2	RW	0x0	vif0_ddr_phase Video Interface DDR phase mode 1'b0: positive edge first 1'b1: negative edge first
1	RW	0x0	vif0_ddr_en Video Interface SDR/DDR select 0: disable 1: enable

Bit	Attr	Reset Value	Description
0	RW	0x0	vif0_en Video Interface enable 0: disable 1: enable

VIF_VIF0_REG_1

Address: Operational Base + offset (0x0004)

vif0 setting register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vif0_frame_vst frame vertical start point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif0_frame_hst frame horizontal start point

VIF_VIF0_REG_2

Address: Operational Base + offset (0x0008)

vif0 horizontal timing setting

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vif0_hs_end horizontal timing sync end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif0_htotal horizontal timing total period

VIF_VIF0_REG_3

Address: Operational Base + offset (0x000c)

Horizontal timing active

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vif0_hact_end horizontal timing active end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif0_hact_st horizontal timing active start point

VIF_VIF0_REG_4

Address: Operational Base + offset (0x0010)

vertical timing

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vif0_vs_end vertical timing sync end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif0_vtotal vertical timing total period

VIF_VIF0_REG_5

Address: Operational Base + offset (0x0014)
vertical timing active

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vif0_vact_end vertical timing active end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif0_vact_st vertical timing active start point

VIF_VIF1_REG_0

Address: Operational Base + offset (0x0018)
vif1 ctrl register

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:4	RO	0x0	reserved
3	RW	0x0	vif1_diffclk_en Video Interface DDR clock mode 1'b0: single clock 1'b1: differential clocks

Bit	Attr	Reset Value	Description
2	RW	0x0	vif1_ddr_phase Video Interface DDR phase mode 1'b0: positive edge first 1'b1: negative edge first
1	RW	0x0	vif1_ddr_en Video Interface SDR/DDR select 0: disable 1: enable
0	RW	0x0	vif1_en Video Interface enable 0: disable 1: enable

VIF_VIF1_REG_1

Address: Operational Base + offset (0x001c)
vif1 setting register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vif1_frame_vst frame vertical start point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif1_frame_hst frame horizontal start point

VIF_VIF1_REG_2

Address: Operational Base + offset (0x0020)
vif1 horizontal timing setting

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vif1_hs_end horizontal timing sync end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif1_htotal horizontal timing total period

VIF_VIF1_REG_3

Address: Operational Base + offset (0x0024)
horizontal timing active

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved

Bit	Attr	Reset Value	Description
27:16	RW	0x000	vif1_hact_end horizontal timing active end point
11:0	RW	0x000	vif1_hact_st horizontal timing active start point

VIF_VIF1_REG_4

Address: Operational Base + offset (0x0028)

vertical timing

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	vif1_vs_end vertical timing sync end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif1_vtotal vertical timing total period

VIF_VIF1_REG_5

Address: Operational Base + offset (0x002c)

vertical timing active

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	vif1_vact_end vertical timing active end point
15:12	RO	0x0	reserved
11:0	RW	0x000	vif1_vact_st vertical timing active start point

Scaler_SCL_REG_0

Address: Operational Base + offset (0x0030)

scaler ctrl register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:9	RO	0x0	reserved
8	RW	0x0	scl_ver_down_mode 0: Bilinear 1: Proprietary averaging filter
7	RW	0x0	scl_hor_down_mode 0: Bilinear 1: Proprietary averaging filter
6:5	RW	0x0	scl_bic_coe_sel 0: precise(a=-0.75); 1: spline(a=0); 2: catrom(a=-0.5); 3: mitchell(a=-1/3);
4:3	RW	0x0	scl_ver_mode 0: no scale; 1: scale up; 2: scale down;
2:1	RW	0x0	scl_hor_mode 0: no scale; 1: scale up; 2: scale down;
0	RW	0x0	scl_en 0: scaler disable; 1: scaler enable;

Scaler_SCL_REG_1

Address: Operational Base + offset (0x0034)

scaler horizontal/vertical factor register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	scl_v_factor (1)scaling up: $(V_{in_act}-1)/(V_{out_act}-1)*2^{16}$; (2)scaling down(bilinear): if $(H_{in_act}-1)/(V_{out_act}-1) > 2.0$, $(V_{in_act}-1)/(V_{out_act}-1)*2^{14}$; else $(V_{in_act}-2)/(V_{out_act}-1)*2^{14}$; (3)scaling down(average): $(V_{out_act})/(V_{in_act}-1)*2^{16}$;
15:0	RW	0x0000	scl_h_factor (1)scaling up: $(H_{in_act}-1)/(H_{out_act}-1)*2^{16}$; (2)scaling down(bilinear): $(H_{in_act}-1)/(H_{out_act}-1)*2^{14}$ if $(H_{in_act}-1)/(H_{out_act}-1) > 2.0$, $(H_{in_act}-1)/(H_{out_act}-1)*2^{14}$; else $(H_{in_act}-2)/(H_{out_act}-1)*2^{14}$ (3)scaling down(average): $(H_{out_act})/(H_{in_act}-1)*2^{16}$;

Scaler_SCL_REG_2

Address: Operational Base + offset (0x0038)
scaler output scanning start setting register

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_frame_vst scaler dsp frame v start point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_frame_hst scaler dsp frame h start point

Scaler_SCL_REG_3

Address: Operational Base + offset (0x003c)
scaler output scanning horizontal timing

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dsp_hs_end scaler dsp hs end
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_htotal scaler dsp htotal

Scaler_SCL_REG_4

Address: Operational Base + offset (0x0040)
scaler output horizontal active window

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_hact_end scaler dsp horizontal active end point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hact_st scaler dsp horizontal active start point

Scaler_SCL_REG_5

Address: Operational Base + offset (0x0044)
scaler output scanning vertical timing

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved
23:16	RW	0x00	dsp_vs_end scaler dsp vs end
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vtotal scaler dsp vtotal

Scaler_SCL_REG_6

Address: Operational Base + offset (0x0048)
scaler output vertical active window

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vact_end scaler dsp vertical active end point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vact_st scaler dsp vertical active start point

Scaler_SCL_REG_7

Address: Operational Base + offset (0x004c)
scaler output horizontal border window

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_hbor_end scaler dsp horizontal border end point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_hbor_st scaler dsp horizontal border start point

Scaler_SCL_REG_8

Address: Operational Base + offset (0x0050)

scaler output vertical border window

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27:16	RW	0x000	dsp_vbor_end scaler dsp vertical border end point
15:12	RO	0x0	reserved
11:0	RW	0x000	dsp_vbor_st scaler dsp vertical border start point

FRC_REG_0

Address: Operational Base + offset (0x0054)

dither frc control

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable When bit 16=1, bit 0 can be written by software. When bit 16=0, bit 0 cannot be written by software; When bit 17=1, bit 1 can be written by software. When bit 17=0, bit 1 cannot be written by software; When bit 31=1, bit 15 can be written by software. When bit 31=0, bit 15 cannot be written by software;
15:7	RO	0x0	reserved
6	RW	0x0	frc_den_inv FRC output den invert enable
5	RW	0x0	frc_sync_inv FRC output vsync/hsync invert enable
4	RW	0x0	frc_dclk_inv FRC output dclk invert enable
3	RW	0x0	frc_out_zero hsync/vsync/den output zeros
2	RW	0x0	frc_out_mode 0: RGB24bit 1: RGB18bit
1	RW	0x0	frc_dither_mode Field0000 Abstract 0: FRC 1: Hi-FRC

Bit	Attr	Reset Value	Description
0	RW	0x0	frc_dither_en FRC dither enable RGB888 to RGB666

CRU_CRU_CLKSEL0_CON

Address: Operational Base + offset (0x0058)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable cru_clkssel0_con_mask cru_clkssel0 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15:10	RO	0x0	reserved
9:8	RW	0x10	cfg_pll1in_sel pll1 clk in select pll1in_sel PLL1 clock pll source selection 2'b00:select the div clock from lcdc0_dclkp 2'b01:select the div clock from lcdc1_dclkp 2'b10:select the clk in 12 clock
7:6	RW	0x10	cfg_pll0in_sel pll0 clk in select pll0in_sel PLL0 clock pll source selection 2'b00:select the div clock from lcdc0_dclkp 2'b01:select the div clock from lcdc1_dclkp 2'b10:select the clk in 12 clock
5:3	RW	0x0	cfg_lcdc1_div Control mux_lcdc1 divider frequency lcdc1_div_con Control LCDC1 input clock divider frequency $\text{mux_lcdc1} = \text{lcdc1_dclkp} / (\text{cfg_lcdc1_div} + 1)$

Bit	Attr	Reset Value	Description
2:0	RW	0x0	cfg_lcdc0_div Control mux_lcdc0 divider frequency lcdc0_div_con Control LCDC0 input clock divider frequency $\text{mux_lcdc0} = \text{lcdc0_dclkp} / (\text{cfg_lcdc0_div} + 1)$

CRU_CRU_CLKSEL1_CON

Address: Operational Base + offset (0x005c)
 acodec/scaler clk cfg

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable cru_clkssel1_con_mask cru_clkssel1 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15:13	RO	0x0	reserved
12	RW	0x0	cfg_lcdcclk_gaten lcdclk_gating lcdc clock gating sel which source from dither clock when high,gating the lcdc(io intf) clock
11	RW	0x0	cfg_lcdc1clk_gaten lcdc1clk_gating lcdc1 clock gating sel which source from dither clock when high,gating the lcdc1(io intf) clock
10	RW	0x0	cfg_mipiclk_gaten mipiclk_gating mipi clock gating sel which source from dither clock when high,gating the mipi clock
9	RW	0x0	cfg_lvdsclk_gaten lvdsclk_gating lvds clock gating sel which source from dither clock when high,gating the lvds clock

Bit	Attr	Reset Value	Description
8	RW	0x0	cfg_hdmiclk_gaten hdmiclk_gating hdmi clock gating sel when high,gating the hdmi clock
7:5	RW	0x0	cfg_scaler_div Control scaler clk divider frequency scaler_clk_div_con Control scaler clock divider frequency scaler_clk=scaler_muxin/(cfg_scaler_div+1)
4	RW	0x0	cfg_scaler_gaten scaler clock gating scaler_gating scaler clock gating sel when high,gating the scaler clock
3	RW	0x0	cfg_scaler_sel scaler clk in select scaler clock source sel scaler source selection 1'b0:select the clock from the output clock of PLL0 1'b1:select the clock from the output clock of PLL1
2	RW	0x0	cfg_codec_gaten codec clock gating codecin_gating ACODEC mclk clock source gating sel when high,gating the acodec mclk clock
1:0	RW	0x0	cfg_codec_sel acodec clk in select codecin_sel ACODEC mclk clock source selection 2'b00:select the clock from the output clock of PLL0 2'b01:select the clock from the output clock of PLL1 2'b10:select the clkin 12 clock

CRU_CRU_CLKSEL2_CON

Address: Operational Base + offset (0x0060)

acodec frac div

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:0	RW	0x00000000	cfg_codec_div acodec clk in select acodec clk frac div $acodec_clk = acodec_clkin / (cfg_codec_div + 1)$ note: the input source clock / the output clock > 20

CRU_CRU_CLKSEL3_CON

Address: Operational Base + offset (0x0064)

vif0/vif1/hdmi/mipi clock cfg

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable bit0~15 write enable cru_clksel3_con_mask cru_clksel3 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RW	0x0	cfg_scalerin_sel scalerin clk in select scalerin clock source sel scalerin source selection 1'b0: source from vedio_inf0_clk 1'b1: source from vedio_inf1_clk
14	RW	0x1	cfg_dither_sel dither clk in select dither clock source sel dither source selection 0: source from vedio_inf0_clk 1: source from scaler_clk
13:12	RW	0x0	cfg_hdmi_sel hdmi clk in select hdmi clock source sel hdmi source selection 00: source from vedio_inf1_clk 01: source from scaler_clk 10: source from vedio_inf0_clk

Bit	Attr	Reset Value	Description
11:9	RW	0x0	cfg_vedioinf1_div Control vedioinf1 clk divider frequency vedioinf1_clk_div_con Control vedioinf1 clock divider frequency $\text{vedioinf1_clk} = \text{vedioinf1_muxin} / (\text{cfg_vedioinf1_div} + 1)$
8	RW	0x0	cfg_vedioinf1_gaten vedioinf1 clock gating vedioinf1clk_gating vedioinf1clk clock gating sel when high,gating the vedioinf1 clock
7	RW	0x1	cfg_vif1_bypass vif1 clock bypass enable 1:bypass vif1 module,clock select lcdc1_dclkp 0:don't bypass vif1 module,clock select vif1_clk
6	RW	0x0	cfg_vedioinf1_sel vedioinf1 clk in select vedioinf1 clock source sel vedioinf1(vif interface 1) source selection 1'b0:select the clock from the output clock of PLL0 1'b1:select the clock from the output clock of PLL1
5:3	RW	0x0	cfg_vedioinf0_div Control vedioinf0 clk divider frequency vedioinf0_clk_div_con Control vedioinf0 clock divider frequency $\text{vedioinf0_clk} = \text{vedioinf0_muxin} / (\text{cfg_vedioinf0_div} + 1)$
2	RW	0x0	cfg_vedioinf0_gaten vedioinf0 clock gating vedioinf0clk_gating vedioinf0clk clock gating sel when high,gating the vedioinf0 clock
1	RW	0x1	cfg_vif0_bypass vif0 clock bypass enable 1:bypass vif0 module,clock select lcdc0_dclkp 0:don't bypass vif0 module,clock select vif0_clk

Bit	Attr	Reset Value	Description
0	RW	0x0	cfg_vedioinf0_sel vedioinf0 clk in select vedioinf0 clock source sel vedioinf0(vif interface 0) source selection 1'b0:select the clock from the output clock of PLL0 1'b1:select the clock from the output clock of PLL1

CRU_CRU_PLL0_CON0

Address: Operational Base + offset (0x0068)

PLL0 control register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bit_write_mask cru_pll0_con0_mask cru_pll0_con0 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RW	0x0	bp PLL0 bypass
14:12	RW	0x1	postdiv1 PLL0 factor postdiv1
11:0	RW	0x028	fbdiv PLL0 factor fbdiv

CRU_CRU_PLL0_CON1

Address: Operational Base + offset (0x006c)

PLL0 control register1

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bit_write_mask cru_pll0_con1_mask cru_pll0_con1 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RO	0x0	lock PLL0 lock status
14:11	RO	0x0	reserved
10	RW	0x0	pd PLL0 software power down
9	RW	0x1	dsmpd when 1, PLL0 work at integer mode when 0, PLL0 work at frac mode
8:6	RW	0x1	postdiv2 PLL0 factor postdiv2
5:0	RW	0x01	refdiv PLL factor refdiv

CRU_CRU_PLL0_CON2

Address: Operational Base + offset (0x0070)

PLL0 control register1

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RW	0x1	fout4phasepd PLL0 4 phase clock power down, active high
26	RW	0x0	foutvcopd PLL0 buffered VCO clock power down, active high
25	RW	0x0	foutpostdivpd PLL0 post divide power down, active high
24	RW	0x0	dacpd PLL0 cancellation DAC power down, active high
23:0	RW	0x000000	frac PLL0 factor frac

CRU_CRU_PLL1_CON0

Address: Operational Base + offset (0x0074)

PLL1 control register0

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bit_write_mask cru_pll1_con0_mask cru_pll1_con0 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RW	0x0	bp PLL1 bypass
14:12	RW	0x1	postdiv1 PLL1 factor postdiv1
11:0	RW	0x028	fbdiv PLL1 factor fbdiv

CRU_CRU_PLL1_CON1

Address: Operational Base + offset (0x0078)

PLL1 control register1

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bit_write_mask cru_pll1_con1_mask cru_pll1_con1 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RO	0x0	lock PLL1 lock status
14:11	RO	0x0	reserved
10	RW	0x0	pd PLL1 software power down
9	RW	0x1	dsmpd when 1, PLL1 work at interger mode when 0, PLL1 work at frac mode
8:6	RW	0x1	postdiv2 PLL1 factor postdiv2

Bit	Attr	Reset Value	Description
5:0	RW	0x01	refdiv PLL1 factor refdiv

CRU_CRU_PLL1_CON2

Address: Operational Base + offset (0x007c)

PLL1 control register1

Bit	Attr	Reset Value	Description
31:28	RO	0x0	reserved
27	RO	0x1	fout4phasepd PLL1 4 phase clock power down, active high
26	RW	0x0	foutvcopd PLL1 buffered VCO clock power down, active high
25	RW	0x0	foutpostdivpd PLL1 post divide power down, active high
24	RW	0x0	dacpd PLL1 cancellation DAC power down, active high
23:0	RW	0x000000	frac PLL1 factor frac

CRU_I2C_CON0

Address: Operational Base + offset (0x0080)

i2c filter cfg register

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x0	cfg_i2c_timeoutp Rising Timeout period for I2C glitch filter
3:0	RW	0x0	cfg_i2c_timeoutf Falling Timeout period register for I2C glitch filter

CRU_LVDS_CON0

Address: Operational Base + offset (0x0084)

lvds config register

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:16	WO	0x0000	bit_write_mask lvds_con0_mask lvds_con0 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RO	0x0	reserved
14	RW	0x0	lvds_con_start_phase dclk_div2 start phase at beginning of hs 0: h_bp width is even,dclk_div2 reset to 0 at beginning of hs 1: h_bp width is odd,dclk_div2 reset to 1 at beginning of hs
13	RW	0x0	lvds_dclk_inv lvds dclk_div2 invert enable,used in dual channel lvds mode 0: no invert 1: invert
12	RW	0x0	lvds_con_cha1ds Channel1 output loading selectpin,combined with bit [11] when configure. {lvds_con_cha0ds,lvds_con_cha1ds}: 2'b00:3pf 2'b01:7pf 2'b10:5pf 2'b11:10pf
11	RW	0x0	lvds_con_cha0ds Channel0 output loading select pin, combined with bit [12] when configure. {lvds_con_cha0ds,lvds_con_cha1ds}: 2'b00:3pf 2'b01:7pf 2'b10:5pf 2'b11:10pf
10	RW	0x0	lvds_con_cha1ttl_en TTL output enable for channel 1 0: output disable 1: output enable

Bit	Attr	Reset Value	Description
9	RW	0x0	lvds_con_cha0ttl_en TTL output enable for channel 0 0: output disable 1: output enable
8	RW	0x0	lvds_con_cha1pd Power down LVDS channel1 0: power down 1: working mode
7	RW	0x0	lvds_con_cha0pd Power down LVDS channel0 0: power down 1: working mode
6	RW	0x0	lvds_con_cbgpd Power down LVDS CBG 0: CBG power down 1: working mode
5	RW	0x1	lvds_con_pllpd Power down LVDS internal PLL 0: working mode 1: power downpll
4	RW	0x0	lvds_con_startsel LVDS start channel select 0: channel0 transmit odd pixel 1: channel0 transmit even pixel
3	RW	0x0	lvds_con_chasel LVDS output channel select 0: just channel0 output 1: channel0 and channel1 output
2	RW	0x0	lvds_con_msbsel LVDS lane input format 0: MSB is on D0. 1: MSB is on D7
1:0	RW	0x0	lvds_con_select LVDS output format 00: 8bit mode format-1 01: 8bit mode format-2 10: 8bit mode format-3 11: 6bit mode

CRU_IO_CON0

Address: Operational Base + offset (0x0088)

IO CFG register pull-up/pull-down/output enable

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bit_write_mask Field0000 Abstract io_con0_mask io_con0 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15	RW	0x0	vif1_syncmode_sel vif0 module sync mode enable 1:enable sync mode 0:disable sync mode
14	RW	0x0	vif0_syncmode_sel vif0 module sync mode enable 1:enable sync mode 0:disable sync mode
13	RW	0x1	i2s1_sdo_outen i2s1 channel output enable 0:enable 1:disable
12	RW	0x1	i2s0_sdo_outen i2s0 channel output enable 0:enable 1:disable
11	RW	0x1	lcdc_oen Field0000 Abstract IO_LCDC_DCLK/VSYNC/HSYNC/DEN/DATA[23:20] output enable 0:enable 1:disable LVDS intf become RGB intf
10	RW	0x1	lcdc1_oen IO_LCDC1_DCLKP/DCLKN/VSYNC/HSYNC/DEN/DATA[23:0] output enable 1:disable 0:enabl,becom RGB intf ,the dither data to the intf

Bit	Attr	Reset Value	Description
9	RW	0x0	lcdc_ren IO_LCDC_DCLK/VSYNC/HSYNC/DEN/DATA[23:20] pull-down enable 0:enable 1:disable
8	RW	0x0	lcdc1_ren IO_LCDC1_DCLKP/DCLKN/VSYNC/HSYNC/DEN/DATA[23:0] pull-down enable 0:enable 1:disable
7	RW	0x0	lcdc0_ren IO_LCDC0_DCLKP/DCLKN/VSYNC/HSYNC/DEN/DATA[23:0] pull-down enable 0:enable 1:disable
6	RW	0x0	hdmi_ren IO_HDMI_I2CSCL/I2CSDA/CEC/HDP pull-up enable 0:enable 1:disable
5	RW	0x0	spdif_ren IO_SPDIF pull-down enable 0:enable 1:disable
4	RW	0x0	i2s1_ren IO_I2S1SDI/I2S1_SDO/I2S1BCLK/I2S1SLRCKRX/I2S1SLRCKTX pull-down enable 0:enable 1:disable
3	RW	0x0	i2s0_ren IO_I2S0SDI[0:3]/I2S0_SDO/I2S0BCLK/I2S0SLRCKRX/I2S0SLRCKTX pull-down enable 0:enable 1:disable
2	RW	0x0	i2c_ren IO_I2C_SCL/IO_I2C_SDA pull-up enable 0:enable 1:disable
1	RW	0x0	int_ren interrupt input pad ,pull-down 0:pull-down 1:pull-up

Bit	Attr	Reset Value	Description
0	RW	0x0	clkin_ren clkin 12M input pad ,pull-down 0:pull-down 1:pull-up

CRU_IO_CON1

Address: Operational Base + offset (0x008c)

IO CFG register schmitt input enable

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	bit_write_mask io_con1_mask io_con1 control write mask When every bit HIGH, enable the writing corresponding bit When every bit LOW, don't care the writing corresponding bit ex: the writing corresponding bit of bit31 is bit15 the writing corresponding bit of bit16 is bit0
15:10	RO	0x3f	reserved
9	RW	0x1	lcdc_ie IO_LCDC_DCLK/VSYNC/HSYNC/DEN/DATA[23:20] schmitt input enable 0:disable 1:enable
8	RW	0x1	lcdc1_ie IO_LCDC1_DCLKP/DCLKN/VSYNC/HSYNC/DEN/DATA[23:0] schmitt input enable 0:disable 1:enable
7	RW	0x1	lcdc0_ie IO_LCDC0_DCLKP/DCLKN/VSYNC/HSYNC/DEN/DATA[23:0] schmitt input enable 0:disable 1:enable
6	RW	0x1	hdmi_ie IO_HDMI_I2CSCL/I2CSDA/CEC/HDP schmitt input enable 0:disable 1:enable

Bit	Attr	Reset Value	Description
5	RW	0x1	spdif_ie IO_SPDIF schmitt input enable 0:disable 1:enable
4	RW	0x1	i2s1_ie IO_I2S1SDI/I2S1_SDO/I2S1BCLK/I2S1SLRCKRX/I2S1SLRCKTX schmitt input enable 0:disable 1:enable
3	RW	0x1	i2s0_ie IO_I2S0SDI[0:3]/I2S0_SDO/I2S0BCLK/I2S0SLRCKRX/I2S0SLRCKTX schmitt input enable 0:disable 1:enable
2	RW	0x1	i2c_ie IO_I2C_SCL/IO_I2C_SDA schmitt input enable 0:disable 1:enable
1	RW	0x1	int_ie Interrupt schmitt input enable 0:disable 1:enable
0	RW	0x1	clkin_ie clkin 12M input pad schmitt input enable 0:disable 1:enable

CRU_pcm2is2_con0

Address: Operational Base + offset (0x0090)
group0

Bit	Attr	Reset Value	Description
31:1	RO	0xf	reserved
0	RW	0x0	pcm2i2s con0

CRU_pcm2is2_con1

Address: Operational Base + offset (0x0094)
group1

Bit	Attr	Reset Value	Description
31:0	RO	0xf	reserved
0	RW	0x0	pcm2i2s con1

CRU_pcm2is2_con2

Address: Operational Base + offset (0x0098)

pcm2is2_con2

Bit	Attr	Reset Value	Description
31:19	RO	0x0	reserved
18:16	RW	0x0	write_bitmask
15:3	RO	0x0	reserved
2	RW	0x0	aps_sel 0:g0 master mode, g1 slave mode 1:g0 slave mode, g1 master mode
1	RW	0x0	aps_clr All logic clear, the configuration information can be change only when this bit is 0
0	RW	0x0	i2s_channel_sel 0:sel i2s channel from I2S0 PAD 1:sel i2s channel from I2S1 PAD

CRU_cfg_misc_con

Address: Operational Base + offset (0x009c)

Register0000 Abstract

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	hdmi_int hdmi interrupt active high valid
19	RO	0x0	mipi_int mipi interrupt active high valid
18	RO	0x0	cfg_pin_micdet1 from codec
17	RO	0x0	cfg_pin_micdet2 from codec
16	RO	0x0	mipi_edpihalt mipi controller traffic control signals
15	RW	0x0	hdmi_hpol_sel hdmi hsync polarity sel 0:don't invert 1:invert
14	RW	0x0	hdmi_vpol_sel hdmi vsync polarity sel 0:don't invert 1:invert

Bit	Attr	Reset Value	Description
13:12	RW	0x0	hdmi_clk_sel hdmi clock source sel hdmi source selection 00:source from vedio_inf1_clk 01:source from scaler_clk 10:source from vedio_inf0_clk
11	RW	0x0	pin_forcetxtstopmode_3 innosilicon mipi phy 0:disable 1:enable
10	RW	0x0	pin_forcetxtstopmode_2 innosilicon mipi phy 0:disable 1:enable
9	RW	0x0	pin_forcetxtstopmode_1 innosilicon mipi phy 0:disable 1:enable
8	RW	0x0	pin_forcetxtstopmode_0 innosilicon mipi phy 0:disable 1:enable
7	RW	0x0	pin_forcerxmode_0 innosilicon mipi phy 0:disable 1:enable
6	RW	0x0	pin_turndisable_0 innosilicon mipi phy 0:disable 1:enable
5	RW	0x0	int_sel interrupt polarity sel 0: high active 1: low active
4	RW	0x0	lvds_con_den_polarity lvds_con_den_polarity lvds den polarity,used in dual channel lvds mode 0: high active 1: low active

Bit	Attr	Reset Value	Description
3	RW	0x0	lvds_con_hs_polarity lvds_con_hs_polarity lvds hsync polarity,used in dual channel lvds mode 0: low active 1: high active
2	RW	0x0	dpicolom mipi controller send color mode sel command 1:8bit mode 0:full mode
1	RW	0x0	dpishutdn mipi controller send shut down command
0	RW	0x0	ad2da_loop codec ad2da_loop signals 1:loop 0:don't loop

2.5I2C Timing Diagram

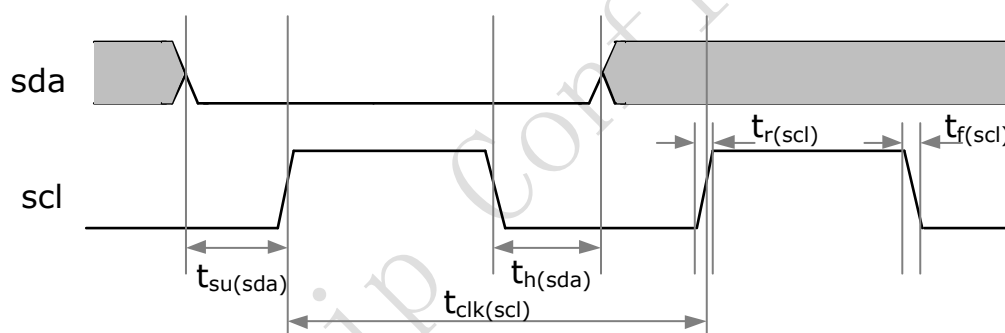


Fig. 2-5 I2C timing diagram

Table 2-2 I2C timing parameters

*timing condition: VCCIO=3.3V,

Parameter		Min.	Typ.	Max.	Unit
100KHz mode					
$t_{clk(scl)}$	SCL clock period	-	10	-	us
$t_{r(scl)}$	rise time for SCL	-	6.5	-	ns
$t_{f(scl)}$	fall time for SCL	-	6.0	-	ns
$t_{h(sda)}$	SDA hold time to falling edge of SCL	-	2.5	-	us
$t_{su(sda)}$	SDA setup time to rising edge of SCL	-	2.5	-	us
400KHz mode					
$t_{clk(scl)}$	SCL clock frequency	-	2.5	-	us
$t_{r(scl)}$	rise time for SCL	-	6.5	-	ns
$t_{f(scl)}$	fall time for SCL	-	6.0	-	ns
$t_{h(sda)}$	SDA hold time to falling edge of SCL	-	0.6	-	us
$t_{su(sda)}$	SDA setup time to rising	-	0.6	-	us

	edge of SCL				
--	-------------	--	--	--	--

2.6 Application Notes

The I2C controller core operation flow chart below is to describe how the software configures and performs an I2C transaction through this I2C controller core. Descriptions are divided into 3 sections, transmit only mode, receive only mode, and mix mode. Users are strongly advised to following.

- Transmit only mode (I2C_CON[2:1]=2'b00)

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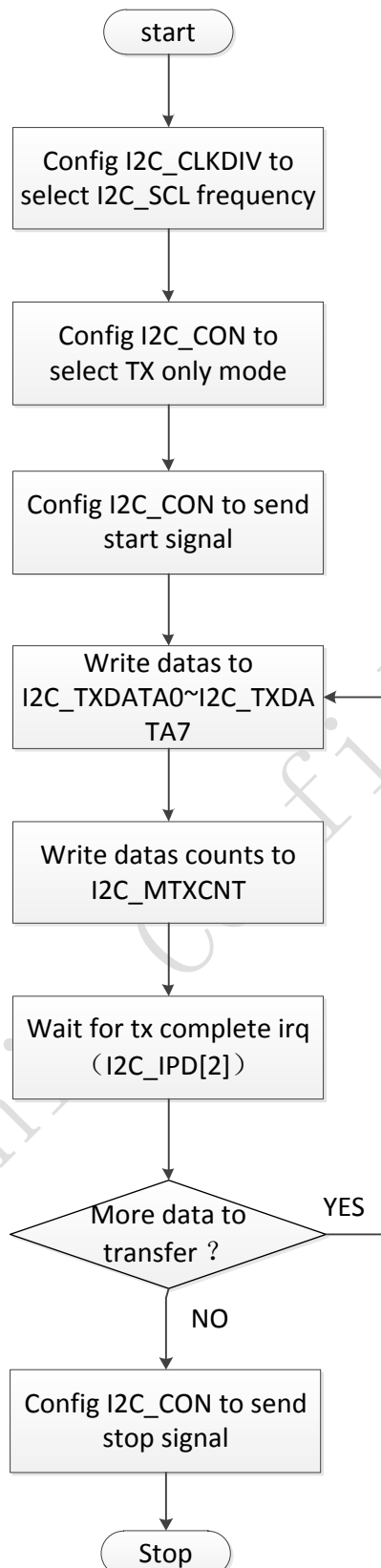


Fig. 2-6I2C Flow chat for tx only mode

- Mix mode (I2C_CON[2:1]=2'b01)

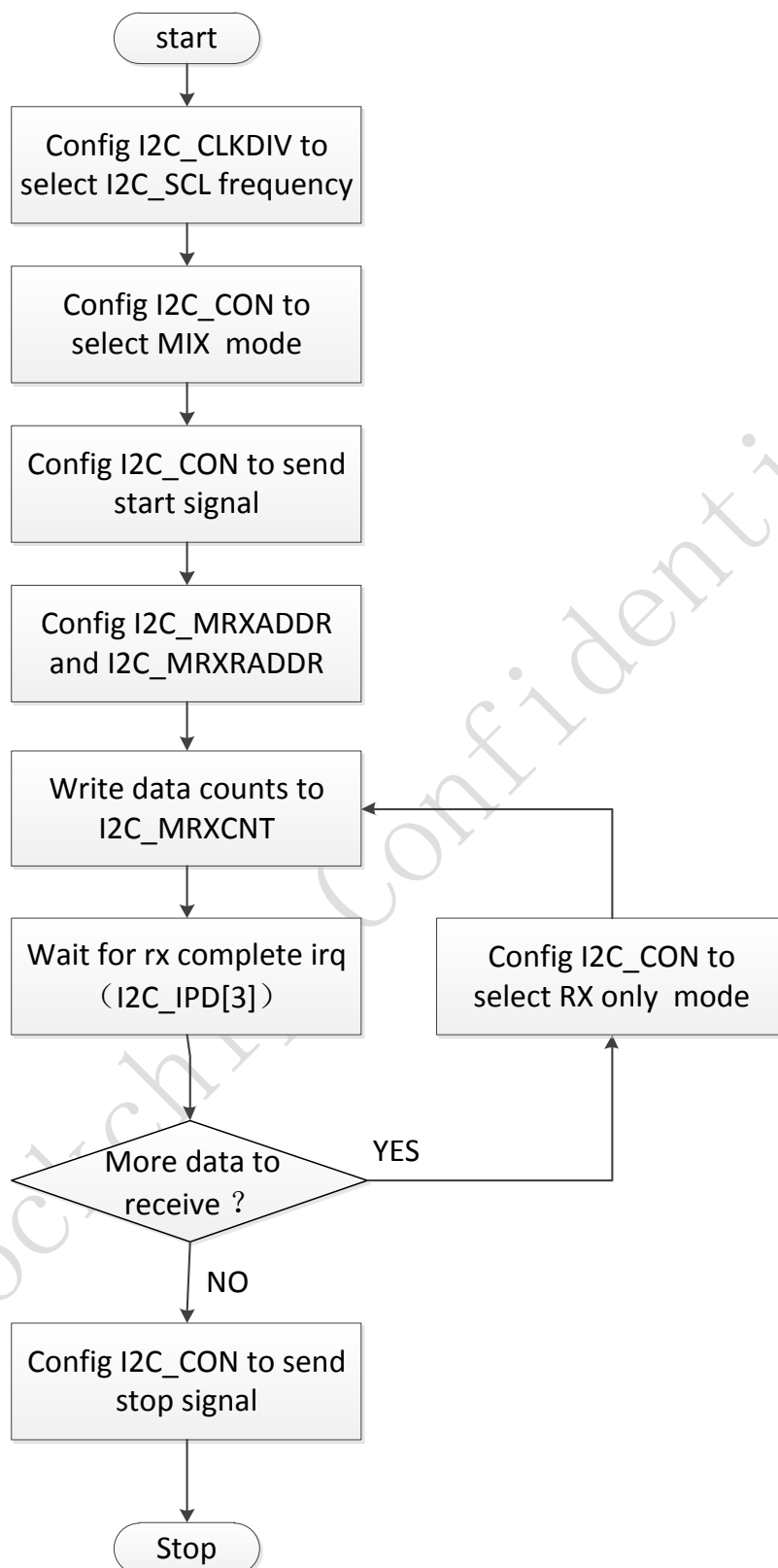


Fig. 2-7I2C Flow chat for mix mode

Chapter 3 CRU (Clock & Reset Unit)

3.1 Overview

The CRU is an module that is designed for generating all of the internal and system clocks, resets of chip. CRU generates system clock from PLL output clock or external clock source, and generate system reset from external power-on-reset.

CRU supports the following features:

- Embedded two PLL
- Flexible selection of clock source
- Supports the respective gating of all clocks

3.2 System Clock Solution

The following diagrams show clock architecture (mux and divider information) in RK61X.

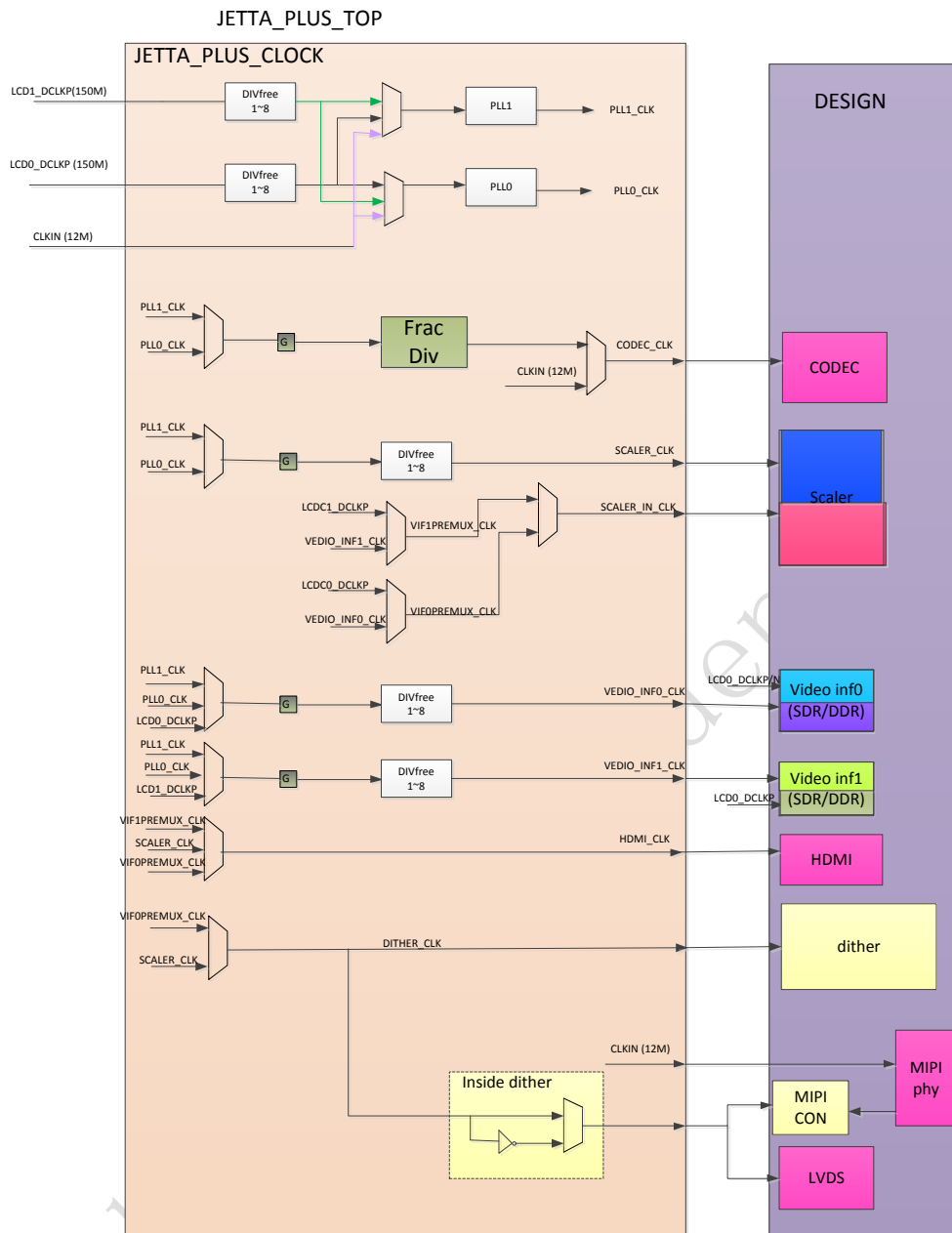


Fig. 3-1Chip Clock Architecture Diagram 1

Description about input clock

The source of input clock in upper diagrams is listed as following Table

Table3-1Input clock description in clock architecture diagram

Input Clock	Source	IO Name
clkin12M	AP I2S master clock output(mclk)	IO_CLKIN
LCDC0_DCLKP	AP LCDC master dclk output(dclk)	IO_LCDC0_D CLKP
LCDC1_DCLKP	AP LCDC master dclk output(dclk)	IO_LCDC1_D CLKP

Description about 2 PLLs selection

From upper diagrams, some clocks can select the source from 2 PLL (pll0_clk and pll1_clk) by the same block name "select from 2PLL", but the selection sequence of each clock may be different, user must refer to the register description in chapter 2.6.

3.3 System Reset Solution

The following diagrams show reset architecture in This device.

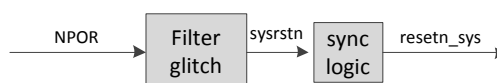


Fig. 3-2 Reset Architecture Diagram

Reset source of each reset signal just includes hardware reset(NPOR), which is from AP. Through the Filter glitch module, it will filter the reset glitch. After that, system reset goes to all other modules for reset-related modules through the sync logic module. The reset signal(resetn_sys) is synchronous de-assert and asynchronous assert.

3.4 Function Description

There are two PLLs in RK61X: PLL0, PLL1, which source from CLKIN, LCDC0_DPCLK and LCDC1_DPCLK. When power on or changing PLL setting, we must force PLL into power down mode.

To maximize the flexibility, some of clocks can select divider source from two PLLs(PLL0 and PLL1).

To provide some specific frequency, another solution is integrated: fractional divider. In order to be sure the performance for divided clock, there is some usage limit, we can only get low frequency and divider factor must be larger than 20.

All clocks can be software gated.

3.5 PLL Introduction

Overview

In RK61X, it uses 1.6GHz PLL for all two PLLs. The 1.6GHz PLL is a general purpose, high-performance PLL-based clock generator. The PLL is a multi-function, general purpose frequency synthesizer. Ultra-wide input and output ranges along with best-in-class jitter performance allow the PLL to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy mixed signal SoC environments. By combining ultra-low jitter output clocks into a low power, low area, widely programmable design, Silicon Creations can greatly simplify a SoC by enabling a single macro to be used for all clocking applications in the system.

1.6GHz PLL supports the following features:

- Input Frequency Range: 1MHz to 800MHz(Integer Mode) and 10MHz to 800MHz(Fractional Mode)

- Output Frequency Range: 1MHz to 1.6GHz
- 24 bit fractional accuracy, and fractional mode jitter performance to nearly match integer mode performance.
- 4:1 VCO frequency range allows PLL to be optimized for minimum jitter or minimum power.
- Isolated analog supply (1.5V to 3.3V) allows for excellent supply rejection in noisy SoC applications.
- Lock Detect Signal indicates when frequency lock has been achieved.

Block diagram

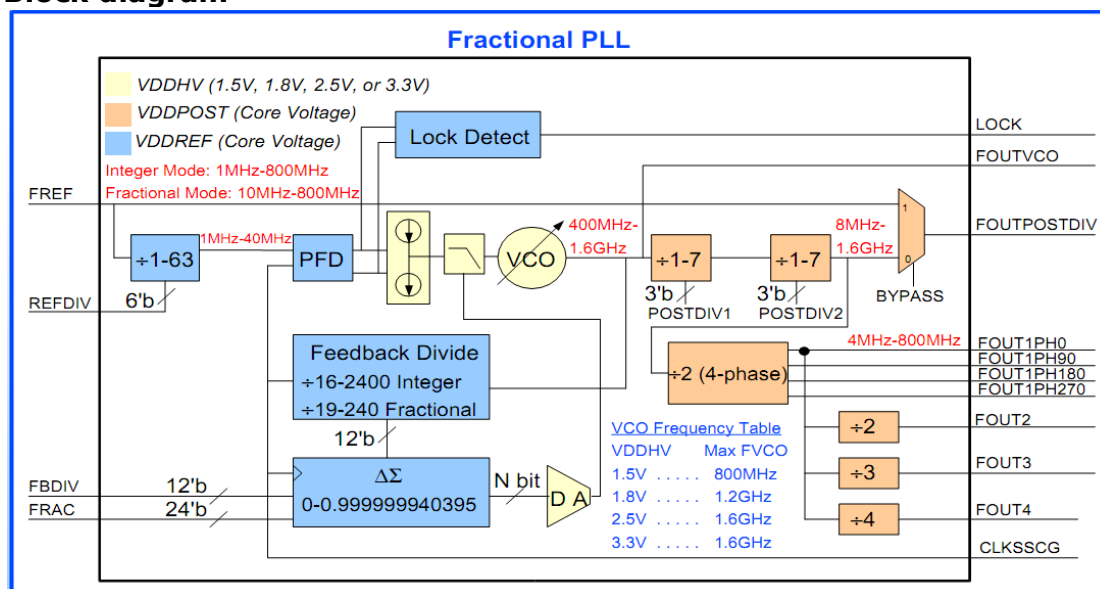


Fig. 3-3PLL Block Diagram

How to calculate the PLL

The Fractional PLL output frequency can be calculated using some simple formulas. These formulas also embedded within the Fractional PLL Verilog model:

If DSMPD = 1 (DSM is disabled, "integer mode")

$$FOUTVCO = FREF / REFDIV * FBDIV$$

$$FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2$$

If DSMPD = 0 (DSM is enabled, "fractional mode")

$$FOUTVCO = FREF / REFDIV * (FBDIV + FRAC / 2^{24})$$

$$FOUTPOSTDIV = FOUTVCO / POSTDIV1 / POSTDIV2$$

Where:

FOUTVCO = Fractional PLL non-divided output frequency

FOUTPOSTDIV = Fractional PLL divided output frequency (output of second post divider)

FREF = Fractional PLL input reference frequency

REFDIV = Fractional PLL input reference clock divider

FVCO = Frequency of internal VCO

FBDIV = Integer value programmed into feedback divide

FRAC = Fractional value programmed into DSM

Changing the PLL Programming

In most cases the PLL programming can be changed on-the-fly and the PLL will simply slew to the new frequency. However, certain changes have the potential to cause glitches on the PLL output clocks. These changes include:

- Switching into or out of BYPASS mode may cause a glitch on FOUTPOSTDIV
- Changing POSTDIV1 or POSTDIV2 may cause a short pulse with width equal to as little as one VCO period on FOUTPOSTDIV
- Changing POSTDIV could cause a shortened pulse on FOUT1PH* or FOUT2/3/4
- Asserting PD or FOUTPOSTDIVPD may cause a glitch on FOUTPOSTDIV

3.6 Register Description

This section describes the control/status registers of the design.

3.6.1 Registers Summary

Name	Offset	Size	Reset Value	Description
CRU_CRU_CLKSEL0_CON	0x0000	W	0x00000000	pll source clock
CRU_CRU_CLKSEL1_CON	0x0004	W	0x00000000	acodec/scaler clk cfg
CRU_CRU_CLKSEL2_CON	0x0008	W	0x00000000	acodec frac div
CRU_CRU_CLKSEL3_CON	0x000c	W	0x00000000	vif0/vif1/hdmi/mipi clock cfg
CRU_CRU_PLL0_CON0	0x0010	W	0x00000000	PLL0 control register0
CRU_CRU_PLL0_CON1	0x0014	W	0x00000000	PLL0 control register1
CRU_CRU_PLL0_CON2	0x0018	W	0x00000000	PLL0 control register1
CRU_CRU_PLL1_CON0	0x001c	W	0x00000000	PLL1 control register0
CRU_CRU_PLL1_CON1	0x0020	W	0x00000000	PLL1 control register1
CRU_CRU_PLL1_CON2	0x0024	W	0x00000000	PLL1 control register1

Notes: **Size:** **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

3.6.2 Detail Register Description

The detail register description refer to chapter 3 I2C.

Chapter 4 VIF(Vedio interface)

4.1 Overview

VIF(vedio interface) is used to LCDC SDR/DDR timing reconstruction.

All the registers can be set through I2C interface.

It supports the following features:

◆ Display interface

- Parallel RGB LCD Interface: 24-bit(RGB888)
- Asynchronous output pixel clock (PLL required)
- Flexible display timing setting
- Support LCDC SDR/DDR timing
- max input width is 4096
- support async mode

4.2 Block Diagram

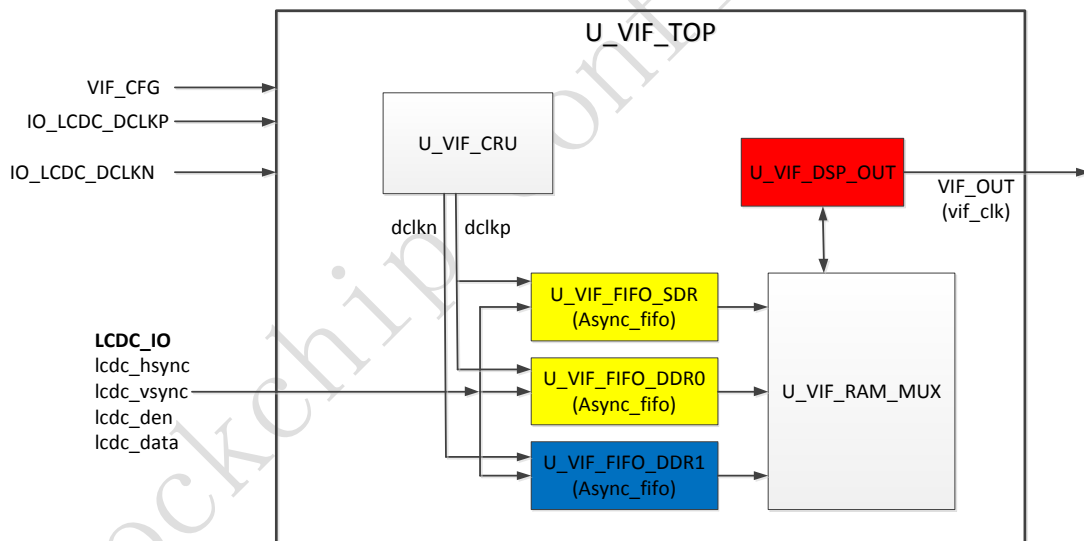


Fig. 4-1 Block diagram of VIF

VIF has three clock domains(dclkp,dclkn,vif_clk).

4.3 Function Description

VIF supports LCDC SDR/DDR timing reconstruction.

For LCDC DDR,VIF supports single DDR clock and differential DDR clocks.

When **cfg_io_con.sync_mode = 0**, the vif don't do a frame synchronous; when **cfg_io_con.sync_mode = 1**, the vif do a frame synchronous.

4.4 Register Description

4.4.1 Registers Summary

Name	Offset	Size	Reset	Description
VIF_REG_0	0xd0	W	0x0	VIF ctrl register
VIF_REG_1	0xd4	W	0x0	scaler factor register
VIF_REG_2	0xd8	W	0x0	scaler output scanning start setting register
VIF_REG_3	0xdc	W	0x0	scaler output scanning horizontal timing
VIF_REG_4	0xe0	W	0x0	scaler output horizontal active window
VIF_REG_5	0xe4	W	0x0	scaler output scanning vertical timing

Notes:

Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** – WORD (32 bits) access

4.4.2 Detail Register Description

Please refer to Chapter 2.4.2.

4.5 LCDC Timing Diagram

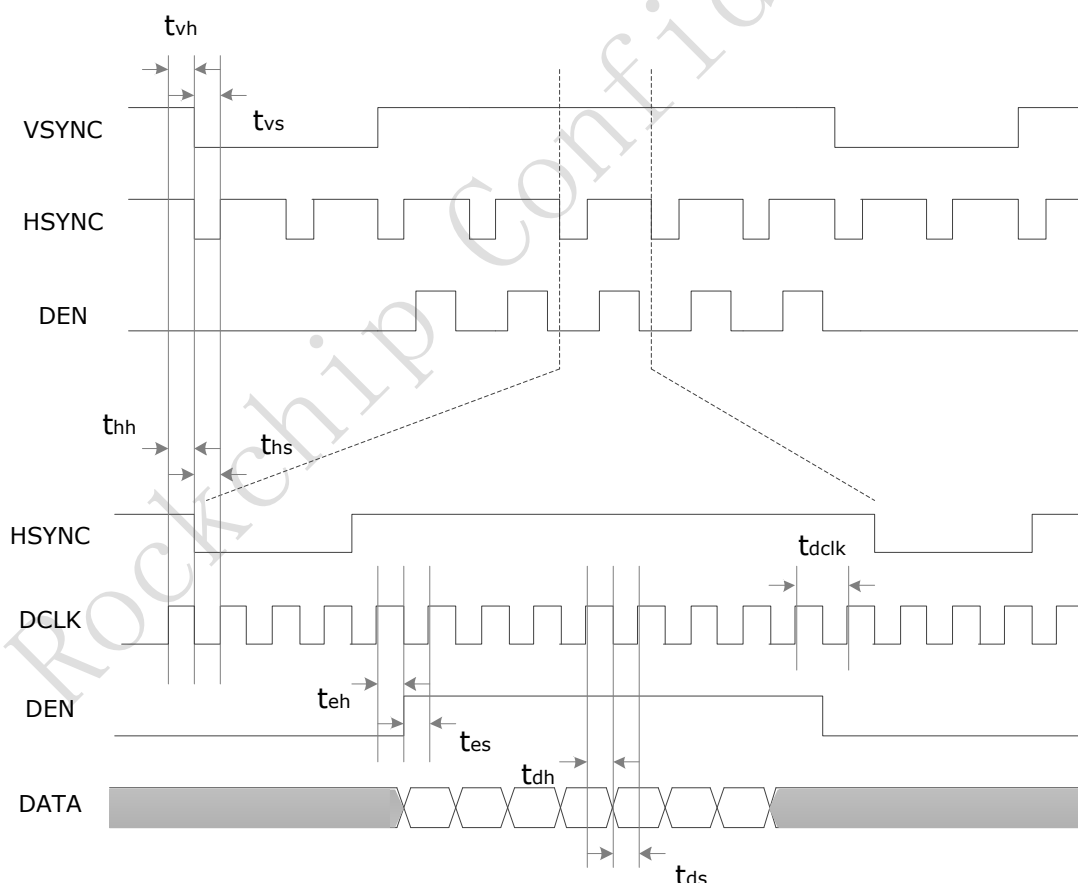


Fig. 4-2 LCDC RGB interface timing (SDR)

Table 4-1 LCDC0 RGB interface (SDR) signal timing constant

*timing condition: VCCIO=3.3V, $C_L \leq 8\text{pF}$, drive strength 8mA

Parameter	Min.	Typ.	Max.	Unit
t_{dclk} Display clock period		5	-	ns

t_{vs}	VSYNC setup to DCLK rising edge	0.44	-	-	ns
t_{vh}	VSYNC hold from DCLK rising edge	-	-	-	ns
t_{hs}	HSYNC setup to DCLK rising edge	0.52	-	-	ns
t_{hh}	HSYNC hold from DCLK rising edge	-	-	-	ns
t_{es}	DEN setup to DCLK rising edge	0.56	-	-	ns
t_{eh}	DEN hold from DCLK rising edge	-0	-	-	ns
t_{ds}	DATA setup to DCLK rising edge	0.64	-	-	ns
t_{dh}	DATA hold from DCLK rising edge	-	-	-	ns

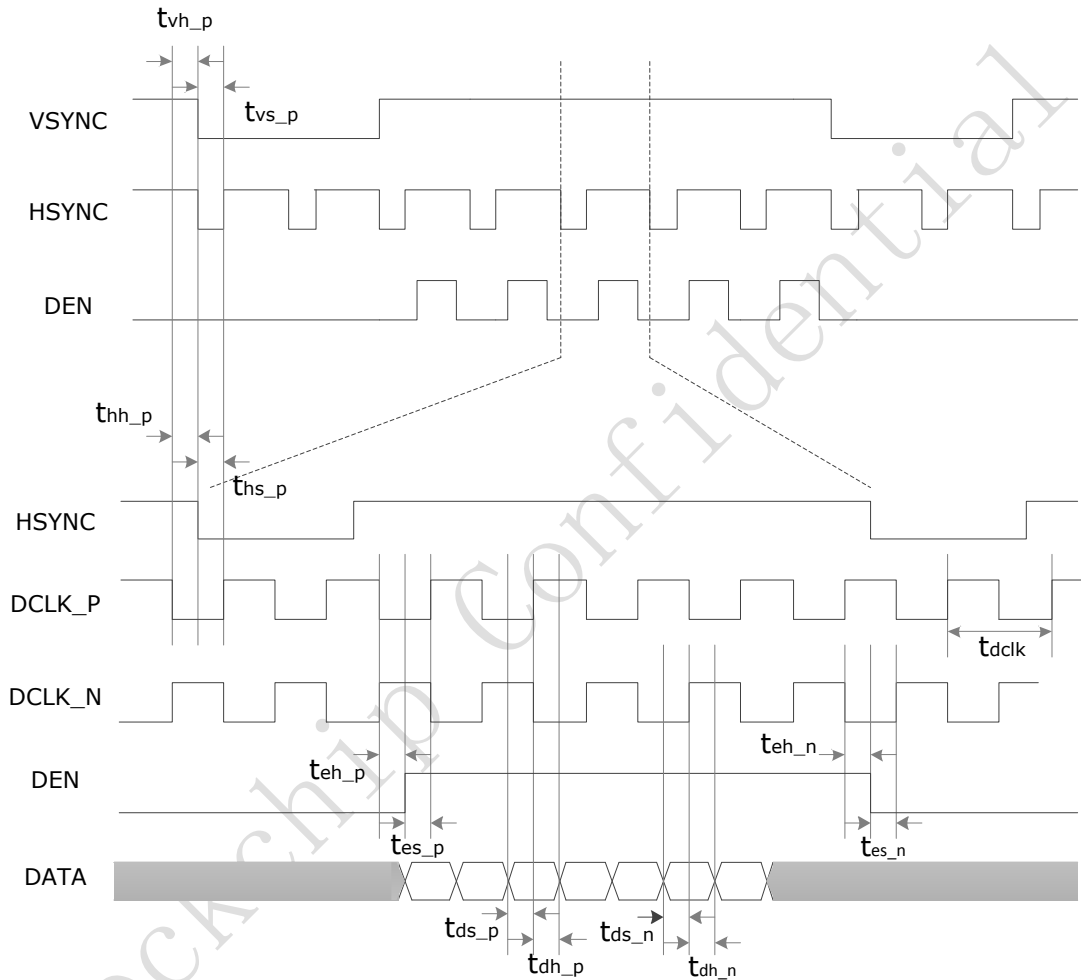


Fig. 4-3 LCDC RGB interface timing (DDR)

Table 4-2 LCDC0 RGB interface (DDR) signal timing constant

*timing condition: VCCIO=3.3V, $C_L \leq 8pF$, drive strength 8mA

Parameter	Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	6.67	-	ns
t_{vs_p}	VSYSNC setup to DCLK_P rising edge	0.84	-	ns
t_{vh_p}	VSYSNC hold from DCLK_P rising edge	-	-	ns
t_{hs_p}	HSYSNC setup to DCLK_P rising edge	0.61	-	ns
t_{hh_p}	HSYSNC hold from DCLK_P rising edge	-	-	ns
t_{es_p}	DEN setup to DCLK_P rising edge	0.88	-	ns
t_{eh_p}	DEN hold from DCLK_P rising edge	-	-	ns
t_{es_n}	DEN setup to DCLK_N rising edge	0.8	-	ns
t_{eh_n}	DEN hold from DCLK_N rising edge	-1	-	ns

t_{ds_n}	DATA setup to DCLK_P rising edge	0.85	-	-	ns
t_{dh_n}	DATA hold from DCLK_P rising edge	-	-	-	ns
t_{ds_p}	DATA setup to DCLK_N rising edge	0.91	-	-	ns
t_{dh_p}	DATA hold from DCLK_N rising edge	-	-	-	ns

Table 4-3 LCDC1 RGB interface (SDR) signal timing constant

*timing condition: VCCIO=3.3V, $C_L \leq 8pF$, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	-	5	-	ns
t_{vs}	VSYNC setup to DCLK falling edge	0.36	-	-	ns
t_{vh}	VSYNC hold from DCLK falling edge	-	-	-	ns
t_{hs}	HSYNC setup to DCLK falling edge	0.42	-	-	ns
t_{hh}	HSYNC hold from DCLK falling edge	-	-	-	ns
t_{es}	DEN setup to DCLK falling edge	0.45	-	-	ns
t_{eh}	DEN hold from DCLK falling edge	-	-	-	ns
t_{ds}	DATA setup to DCLK falling edge	0.61	-	-	ns
t_{dh}	DATA hold from DCLK falling edge	-	-	-	ns

Table 4-4 LCDC1 RGB interface (DDR) signal timing constant

*timing condition: VCCIO=3.3V, $C_L \leq 8pF$, drive strength 8mA

Parameter		Min.	Typ.	Max.	Unit
t_{dclk}	Display clock period	-	6.67	-	ns
t_{vs_p}	VSYNC setup to DCLK_P rising edge	0.69	-	-	ns
t_{vh_p}	VSYNC hold from DCLK_P rising edge	-	-	-	ns
t_{hs_p}	HSYNC setup to DCLK_P rising edge	0.49	-	-	ns
t_{hh_p}	HSYNC hold from DCLK_P rising edge	-	-	-	ns
t_{es_p}	DEN setup to DCLK_P rising edge	0.65	-	-	ns
t_{eh_p}	DEN hold from DCLK_P rising edge	-	-	-	ns
t_{ds_p}	DEN setup to DCLK_N rising edge	0.8	-	-	ns
t_{dh_p}	DEN hold from DCLK_N rising edge	-	-	-	ns
t_{ds_n}	DATA setup to DCLK_P rising edge	0.72	-	-	ns
t_{dh_n}	DATA hold from DCLK_P rising edge	-	-	-	ns
t_{ds_p}	DATA setup to DCLK_N rising edge	0.67	-	-	ns
t_{dh_p}	DATA hold from DCLK_N rising edge	-	-	-	ns

4.6 Application Notes

4.6.1 Programming Sequence

Assert vif_en after all VIF configuration registers are set.

For the frame synchronous of input/output display frames, there are some Programming requirements for SCALER.

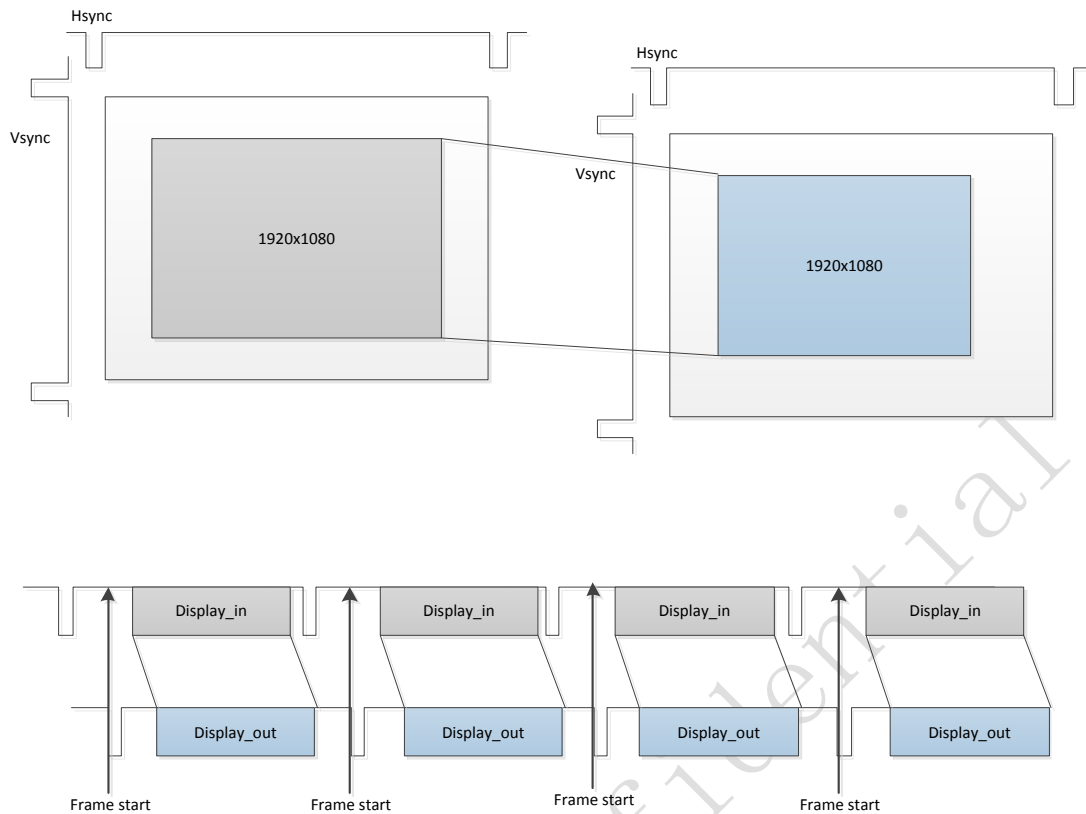


Fig. 4-4 VIF Frame Sync

1. Output Pixel Clock Requirement (VIF PLL setting)

The output pixel clock is asynchronous with input pixel clock to support different display resolution. But the input/output frame frequency should be same because there is no frame buffer in VIF. So there is strict clock requirement for output pixel clock, which is generated from VIF PLL.

The total output active frame period (with horizontal blank period, but without vertical blank period) must be close to the total input active frame period. The difference between them should be less than 15 input active line period (with horizontal blank period).

$$F_{vif} = F_{in}, \text{ for SDR};$$

$$F_{vif} = 2 * F_{in}, \text{ for DDR};$$

Assume that F_{out} is the output pixel clock frequency and F_{in} is the input pixel clock frequency.

$$((dsp_vact_end - dsp_vact_st) * dsp_htotal * 1/F_{out}) \geq (input\ display\ width * (input\ display\ height - 15) / F_{in})$$

$$((dsp_vact_end - dsp_vact_st) * dsp_htotal * 1/F_{out}) \leq (input\ display\ width * (input\ display\ height + 15) / F_{in})$$

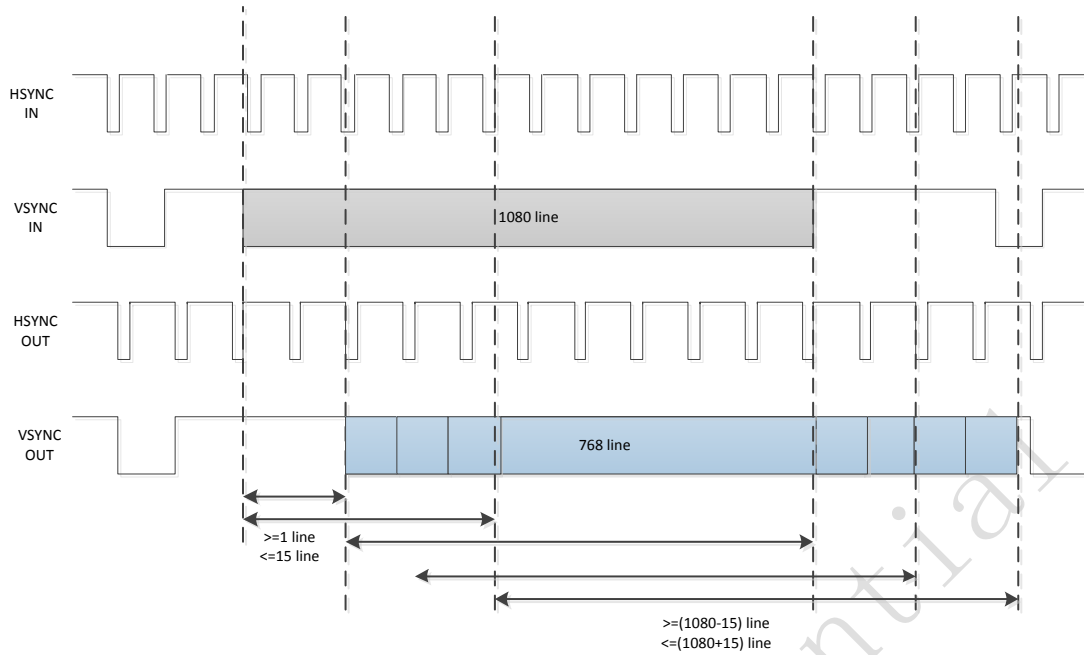


Fig. 4-5 VIF Input/output Active frame period

2. Active pixel start point setting

First, the start point of output active image area should be one line later than the input active image area because of the scaling operation.

usually set $dsp_frame_hst = 1$ and $dsp_frame_vst = 1$.

3. Output frame scanning start point setting

To meet the requirement of active pixel start point, there are dsp_frm_hst/dsp_frm_vst (SCL_REG_2) settings for frame scanning start point adjustment.

The timing delay of output active frame pixel start point behind input active frame pixel start point can be calculated as following equation if their scanning start point is the same ($dsp_frm_hst=0$ and $dsp_frm_vst=0$).

$$\Delta T = (T_{BP_in} - T_{BP_out}),$$

In where T_{BP_in} is the blank period of input frame and T_{BP_out} is the blank period of output frame and.

If the output frame scanning start point is not zero. The timing delay would be:

$$\Delta T = (T_{dsp_frm_vst} + T_{dsp_frm_hst}) + (T_{BP_in} - T_{BP_out})$$

$$T_{dsp_frm_vst} = dsp_frm_vst * input_dsp_htotal * 1/Fin$$

$$T_{dsp_frm_hst} = dsp_frm_hst * 1/Fin$$

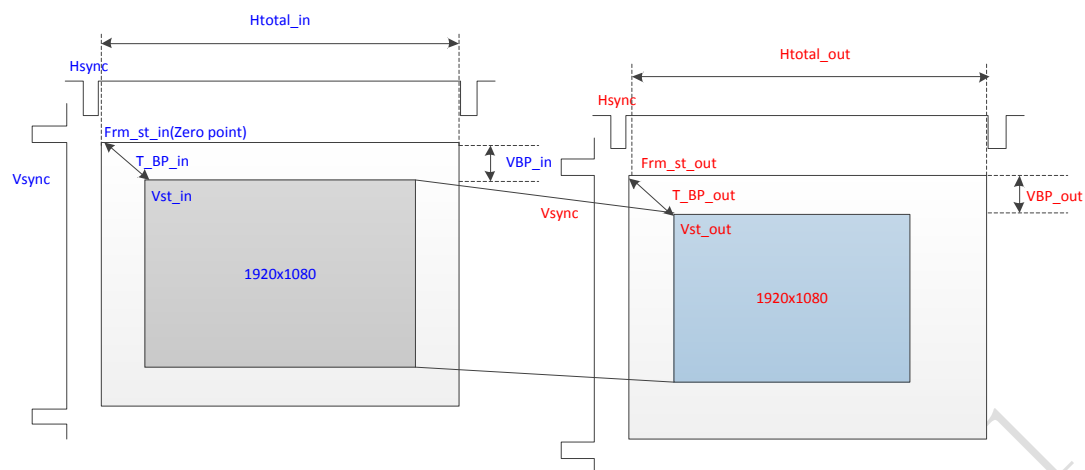


Fig. 4-6 VIF frame scanning start point

Chapter 5 SCALER

5.1 Overview

SCALER is a synchronous parallel RGB frame converter for different resolution. It is used to realize dual display function from one display source.

It can be used like VIF for LCDDC SDR timing reconstruction only.

The input and output of SCALER should be parallel RGB interface. The output timing settings are programmable due to different display resolution. The frame frequency of output frame must be the same with input frame. So the output pixel clock frequency (from PLL) should be set to fit this condition.

All the registers can be set through I2C interface.

It supports the following features:

◆ Display interface

- Parallel RGB LCD Interface: 24-bit(RGB888)
- Asynchronous output pixel clock (PLL required)
- Flexible display timing setting
- Configurable border black area

◆ Imagescaler

- Scaling down
 - Max input resolution: 2560x1600
 - Arbitrary non-integer scaling ratio
 - Support two mode: bilinear and average
 - Max 1/4 scaling ratio for bilinear scaling down
 - Max 1/6 scaling ratio for average scaling down
- Scaling up
 - Max output resolution: 2560x1600
 - Arbitrary non-integer scaling ratio
 - Support four scaling up mode for different effect
 - Max 6 scaling ratio

5.2 Block Diagram

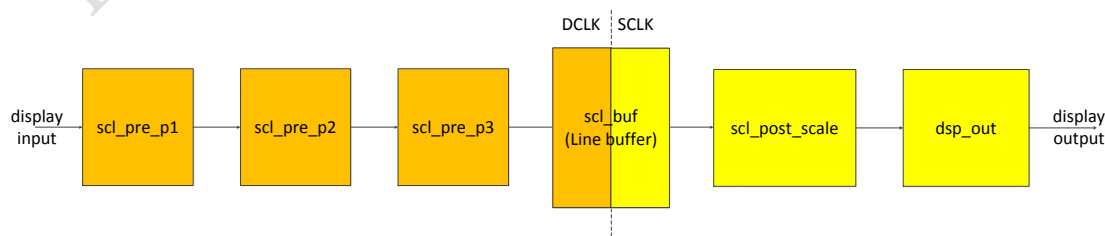


Fig. 5-1 Block diagram of SCALER

The diagram shows that SCALER has two clock domains(DCLK and SCLK).

5.3 Register Description

5.3.1 Registers Summary

Name	Offset	Size	Reset	Description
SCL_REG_0	0xd0	W	0x0	scaler ctrl register
SCL_REG_1	0xd4	W	0x0	scaler factor register
SCL_REG_2	0xd8	W	0x0	scaler output scanning start setting
SCL_REG_3	0xdc	W	0x0	scaler output horizontal timing
SCL_REG_4	0xe0	W	0x0	scaler output horizontal active window
SCL_REG_5	0xe4	W	0x0	scaler output vertical timing
SCL_REG_6	0xe8	W	0x0	scaler output vertical active window
SCL_REG_7	0xec	W	0x0	scaler output horizontal border window
SCL_REG_8	0xf0	W	0x0	scaler output vertical border window

Notes:

Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** – WORD (32 bits) access

5.3.2 Detail Register Description

Please refer to Chapter 2.4.2.

5.4 Application Notes

5.4.1 Scaling Factor Setting

The frame scaling is done by horizontal (X) scaling and vertical (Y) scaling independently. The scaling factor is in SCL_REG_1.

Software calculates the scaling factor value using the following equations:

scl_h_factor

(1) scaling up: $(Hin_act-1)/(Hout_act-1)*2^{16};$

(2) scaling down(bilinear): $(Hin_act-1)/(Hout_act-1)*2^{14}$

if $(Hin_act-1)/(Hout_act-1) > 2.0$, $(Hin_act-1)/(Hout_act-1)*2^{14};$

else $(Hin_act-2)/(Hout_act-1)*2^{14}$

(3) scaling down(average): $(Hout_act)/(Hin_act-1)*2^{16};$

scl_v_factor

(1) scaling up: $(Vin_act-1)/(Vout_act-1)*2^{16};$

(2) scaling down(bilinear):

if $(Vin_act-1)/(Vout_act-1) > 2.0$, $(Vin_act-1)/(Vout_act-1)*2^{14};$

else $(Vin_act-2)/(Vout_act-1)*2^{14};$

(3) scaling down(average): $(Vout_act)/(Vin_act-1)*2^{16};$

In where,

$Hin_act = (dsp_in_hact_end - dsp_in_hact_st);$

$Vin_act = (dsp_in_vact_end - dsp_in_vact_st);$

$Hout_act = (dsp_hact_end - dsp_hact_st);$

$Vout_act = (dsp_vact_end - dsp_vact_st);$

5.4.2 Display Output Timing

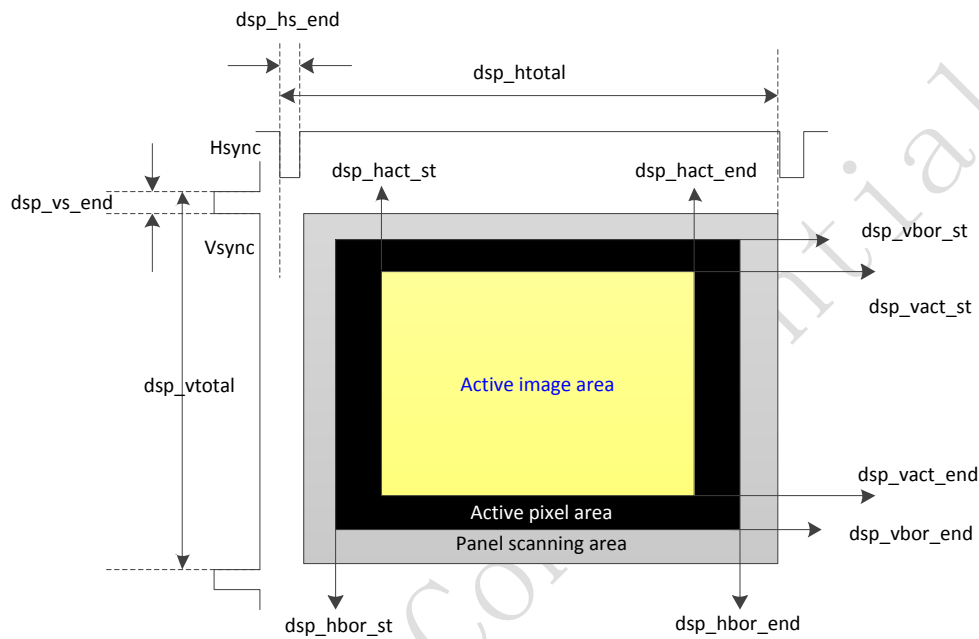


Fig. 5-2 SCALER Output Timing setting

5.4.3 Programming Sequence

Assert `scaler_en` after all scaler configuration registers are set.

For the frame synchronous of input/output display frames, there are some Programming requirements for SCALER.

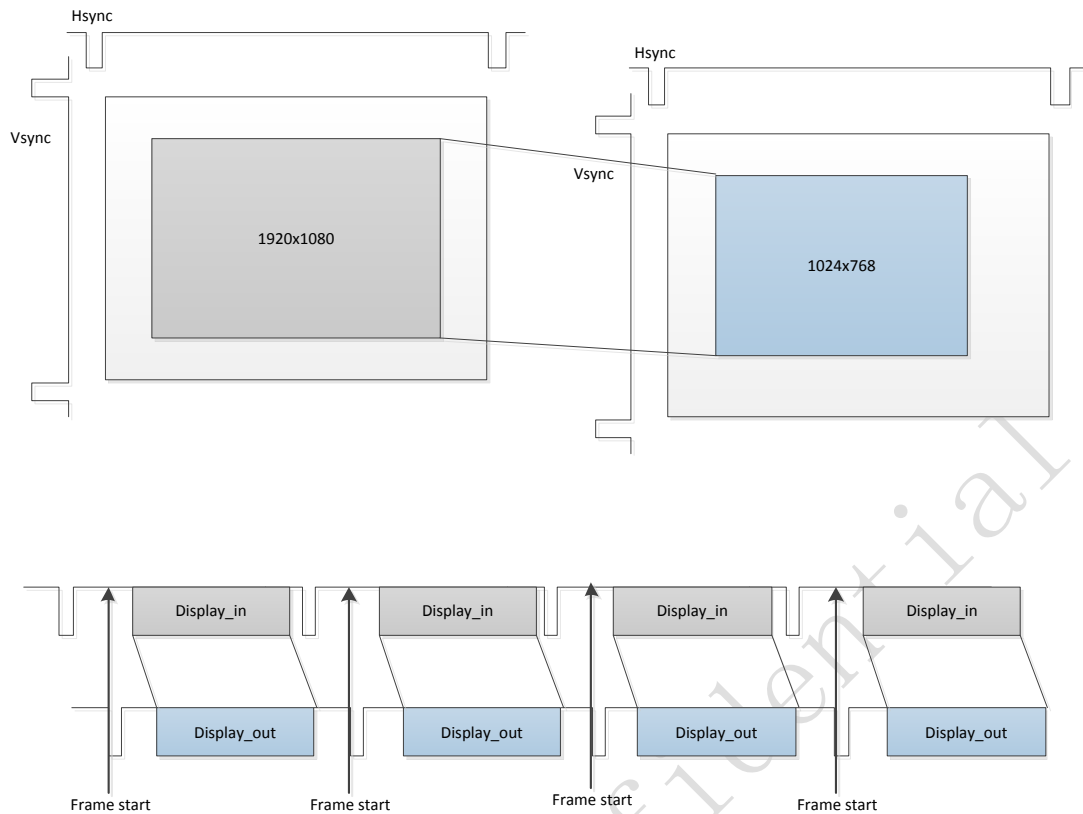


Fig. 5-3 SCALER Frame Sync

4. Output Pixel Clock Requirement (SCALER PLL setting)

The output pixel clock is asynchronous with input pixel clock to support different display resolution. But the input/output frame frequency should be same ($F_{Sin}=F_{Sout}$) because there is no frame buffer in SCALER. So there is strict clock requirement for output pixel clock, which is generated from SCALER PLL.

Assume that F_{out} is the output pixel clock frequency and F_{in} is the input pixel clock frequency.

$$dsp_in_vtotal * dsp_in_htotal * F_{in} = dsp_vtotal * dsp_in_htotal * F_{out};$$

The total output active frame period (include horizontal blank period, but without vertical blank period) must be close to the total input active frame period. The difference between them should be less than X_{max} input active line period (include horizontal blank period).

$$((dsp_vact_end - dsp_vact_st) * dsp_htotal * 1/F_{out}) \geq$$

$$((dsp_in_vact_end - dsp_in_vact_st - X_{max}) * (dsp_in_htotal) * 1/F_{in})$$

$$((dsp_vact_end - dsp_vact_st) * dsp_htotal * 1/F_{out}) \leq$$

$$((dsp_in_vact_end - dsp_in_vact_st + X_{max}) * (dsp_in_htotal) * 1/F_{in})$$

(1) vertical scaling up : $X_{min} = 4$; $X_{max} = 12$;

(2) vertical scaling down (bilinear) :

when $V_scale_ratio < 2$, $X_{min} = 2$; $X_{max} = 14$;

when $V_scale_ratio \geq 2$, $Xmin=4$; $Xmax = 12$;

(3) vertical scaling down (average): $Xmin = V_scale_ratio + 1$; $Xmax = 16 - Xmin$;

(4) no vertical scaling: $Xmin = 2$; $Xmax = 14$;

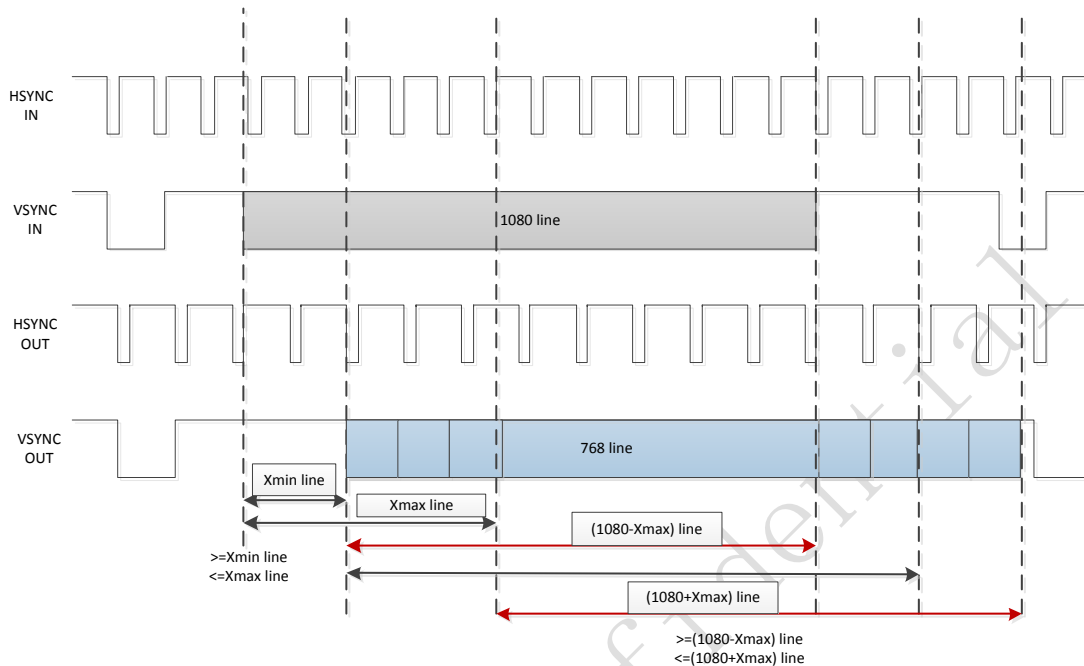


Fig. 5-4 SCALER Input/output Active frame period

5. Active pixel start point setting

First, the start point of output active image area should be $Xmin$ lines later than the input active image area because of the scaling operation.

Second, because of the PLL precision, the total output active frame period would be not equal to the total input active frame period.

(1) So at a setting of the output pixel clock frequency, if the total output active frame period is larger than the total input active frame period. The start point of output active image area should be set after the beginning of $Xmin$ input active pixel line.

$$Xmin * dsp_in_htotal * 1 / Fin \leq \Delta T \leq Xmax * dsp_in_htotal * 1 / Fin$$

Usually, we set ΔT as follow:

$$\Delta T = 7 * dsp_in_htotal * 1 / Fin; \text{ or } \Delta T = 8 * dsp_in_htotal * 1 / Fin;$$

(2) If the total output active frame period is less than the total input active frame period. The start point of output active image area should be set at the beginning of $(Xmax + 1)$ input active pixel line.

$$\Delta T = (X_{\max} * \text{input_dsp_htotal}) * 1 / F_{\text{in}}$$

Usually, we still set ΔT as follow:

$$\Delta T = 7 * \text{dsp_in_htotal} * 1 / F_{\text{in}}; \text{ or } \Delta T = 8 * \text{dsp_in_htotal} * 1 / F_{\text{in}};$$

6. Output frame scanning start point setting

To meet the requirement of active pixel start point, there are $\text{dsp_frm_hst}/\text{dsp_frm_vst}$ (SCL_REG_2) settings for frame scanning start point adjustment.

The timing delay of output active frame pixel start point behind input active frame pixel start point can be calculated as following equation.

$$T_{\text{frm_st}} = (T_{\text{BP_in}} + \Delta T + 3 * \text{dsp_htotal} / F_{\text{out}} - T_{\text{BP_out}});$$

In where,

$$T_{\text{frm_st}} = (\text{dsp_frm_vst} * \text{dsp_in_htotal} + \text{dsp_frm_hst}) / F_{\text{in}};$$

$T_{\text{BP_in}}$ is the blank period of input frame;

$T_{\text{BP_out}}$ is the blank period of output frame and.

if ($T_{\text{frm_st}} < 0$), ΔT should be adjusted as below:

$$T_{\text{frm_st}} = T_{\text{in}} - T_{\text{frm_st}} = \text{dsp_in_vtotal} * \text{dsp_in_htotal} / F_{\text{in}} - \Delta T;$$

then we can calc out dsp_frm_vst and dsp_frm_hst as below:

$$\text{dsp_frm_vst} = \text{floor}((T_{\text{frm_st}} * F_{\text{in}}) / \text{dsp_in_htotal});$$

$$\text{dsp_frm_hst} = (T_{\text{frm_st}} - \text{dsp_frm_vst} * \text{dsp_in_htotal} / F_{\text{in}}) * F_{\text{in}};$$

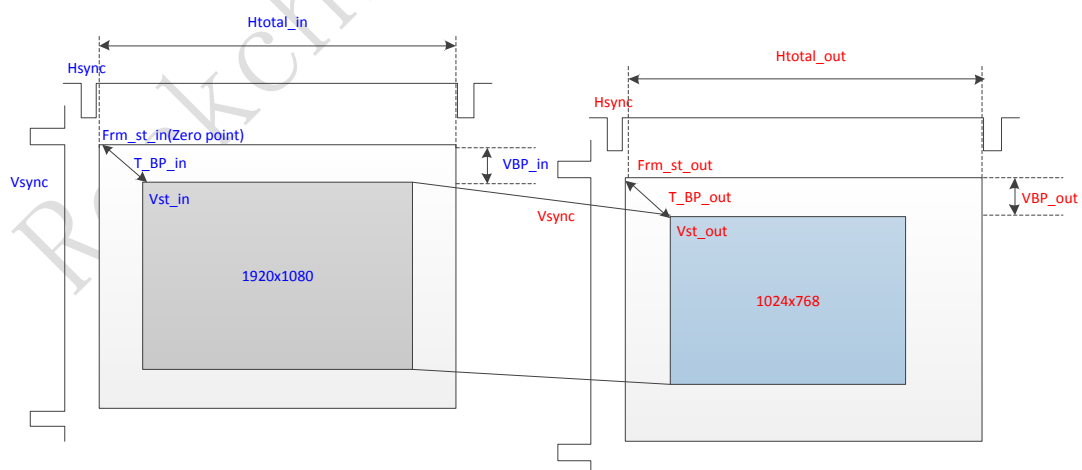


Fig. 5-5 SCALER frame scanning start point

Chapter 6 DITHER

6.1 Overview

DITHER is used for converting 24bit RGB888 to 18bit RGB666 with FRC dither down.

All the registers can be set through I2C interface.

It supports the following features:

◆ **Display interface**

- FRC dither down 24-bit(RGB888) to 18-bit(RGB666)
- output clk/hsync/vsync/den inversion control

6.2 Block Diagram

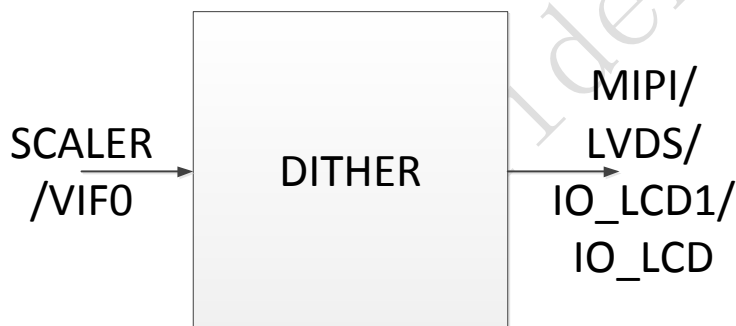


Fig. 6-1Block diagram of DITHER

DITHER has one clock domain,dclk is from scaler or vif0.

6.3 Register Description

6.3.1 Registers Summary

Name	Offset	Size	Reset	Description
FRC_REG_0	0xd0	W	0x0	dither ctrl register

Notes:

Size: **B** – Byte (8 bits) access, **HW** – Half WORD (16 bits) access, **W** –WORD (32 bits) access

6.3.2 Detail Register Description

Please refer to Chapter 2.4.2.

6.4 Application Notes

6.4.1 Programming Sequence

Assert frc_dither_en after all DITHER configuration registers are set.
if JettaB is using LCD1 IO output,frc_dclk_inv should be set as 1.

Chapter 7 MIPI Controller

7.1 Overview

The Display Serial Interface (DSI) is part of a group of communication protocols defined by the MIPI Alliance. The MIPI Controller is a digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI Controller provides an interface between the system and the MIPI D-PHY, allowing the communication with a DSI-compliant display. The MIPI Controller supports one to four lanes for data transmission with MIPI D-PHY.

The MIPI Controller supports the following features:

- Compliant with MIPI Alliance standards
- Support the DPI interface color coding mappings into 24-bit Interface
 - 16 bits per pixel, configurations 1,2,and 3
 - 18 bits per pixel, configurations 1 and 2
 - 24 bits per pixel
- Programmable polarity of all DPI interface signals
- Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels:
 - Up to 2047 vertical active lines
 - Up to 63 vertical back porch lines
 - Up to 63 vertical front porch lines
 - Maximum resolution is limited by available DSI Physical link bandwidth which depends on the number of lanes and maximum speed per lane
- All commands defined in MIPI Alliance Specification for Display Command Set (DCS)
- Interface with MIPI D-PHY following PHY Protocol Interface (PPI), as defined in MIPI Alliance Specification for D-PHY
- Up to four D-PHY Data Lanes
- Bidirectional communication and escape mode support through data lane 0
- Transmission of all generic commands
- ECC and Checksum capabilities
- End of Transmission Packet(EOTp)
- Ultra Low-Power mode
- Fault recovery schemes

7.2 Block Diagram

The following diagram shows the MIPI Controller architecture.

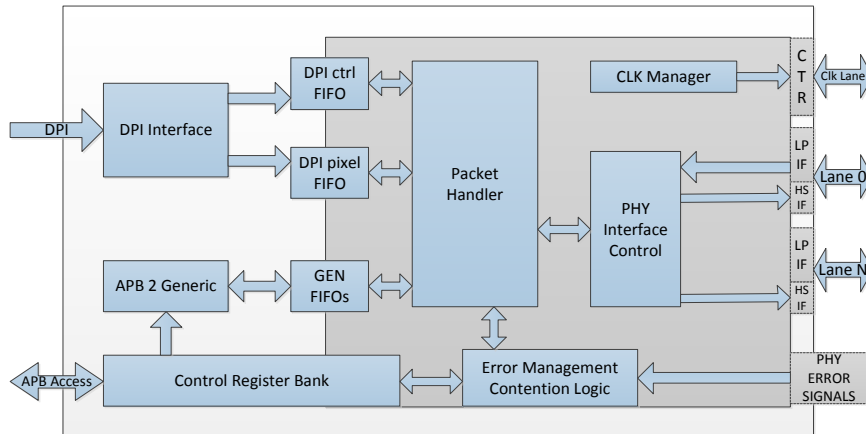


Fig. 7-1 MIPI Controller architecture

The DPI interface captures the data and control signals and conveys them to a FIFO for video control signals and another one for pixel data. This data is then used to build Video packets, then in Video mode.

The Register Bank is accessible through a standard AMBA-APB slave interface, providing access to the MIPI Controller registers for configuration and control. There is also a fully programmable interrupt generator to inform the system about certain events.

The PHY Interface Control is responsible for managing the D-PHY PPI interface. It acknowledges the current operation and enables low-power transmission/reception or a high-speed transmission. It also performs data splitting between available D-PHY lanes for high-speed transmission.

The Packet Handler schedules the activities inside the link. It performs several functions based on the interfaces that are currently DPI and the video transmission mode that is used (burst mode or non-burst mode with sync pulse or sync events). It builds long or short packet generating correspondent ECC and CRC codes. This block also performs the following functions: Packet reception, Validation of packet header by checking the ECC, Header correction and notification for single-bit errors, Termination of reception, Multiple header error notification.

The APB-to-Generic block bridges the APB operations into FIFOs holding the Generic commands. The block interfaces with the following FIFOs: Command FIFO, Write payload FIFO, Read payload FIFO.

The Error Management notifies and monitors the error conditions on the DSI link. It controls the timers used to determine if a timeout condition occurred, performing an internal soft reset and triggering an interruption notification.

7.3 Function Description

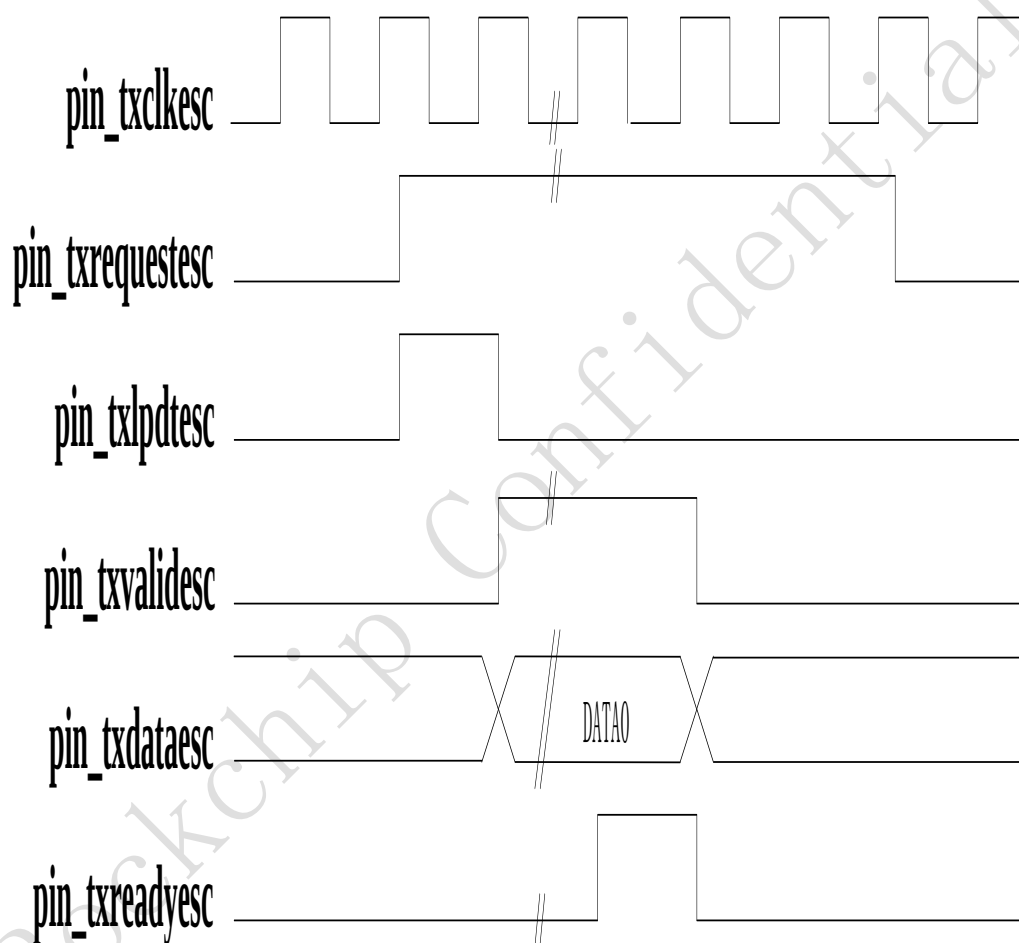
7.3.1 .DPI interface function

The DPI interface follows the MIPI DPI specification with pixel data bus width up to 24 bits. It is used to transmit the information in Video mode in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream. This interface allows sending ShutDown (SD) and ColorMode (CM)

commands, which are triggered directly by writing to the register of CFG_MISC_CON[2:1]. To transfer additional commands(for example, to initialize the display), use another interface such as APB Slave Generic Interface to complement the DPI interface.

The DPI interface captures the data and control signals and conveys them to the FIFO interfaces that transmit them to the DSI link. Two different streams of data are presented at the interface; video control signals and pixel data. Depending on the interface color coding, the pixel data is disposed differently throughout the dpipixdata bus. The following table shows the Interface pixel color coding.

Table 7-1Color table



The DPI interface can be configured to increase flexibility and promote correct usage of this interface for several systems. These configuration options are as follows: Polarity control: All the control signals are programmable to change the polarity depending on system requirements.

After the MIPI Controller reset, DPI waits for the first VSYNC active transition to start signal sampling, including pixel data, and preventing image transmission in the middle of a frame.

If interface pixel color coding is 18 bits and the 18-bit loosely packed stream is disabled, the number of lines programmed in the pixels per lines configuration is a multiple of four. This means that in this mode, the two LSBs in the configuration are always inferred as zero. The specification states that in this

mode, the pixel line size should be a multiple of four.

7.3.2 .APB Slave Generic Interface

The APB Slave interface allows the transmission of generic information in Command mode, and follows the proprietary register interface. Commands sent through this interface are not constrained to comply with the DCS specification, and can include generic commands described in the DSI specification as manufacturer-specific.

The MIPI Controller supports the transmission or write and read command mode packets as described in the DSI specification. These packets are built using the APB register access. The GEN_PLD_DATA register has two distinct functions based on the operation. Writing to this register sends the data as payload when sending a Command mode packet. Reading this register returns the payload of a read back operation. The GEN_HDR register contains the Command mode packet header type and header data. Writing to this register triggers the transmission of the packet implying that for a long Command mode packet, the packet's payload needs to be written in advance in the GEN_PLD_DATA register. The valid packets available to be transmitted through the Generic interface are as follows:

Generic Write Short Packet 0 Parameters

Generic Write Short Packet 1 Parameters

Generic Write Short Packet 2 Parameter

Generic Write Short Packet 0 Parameter

Generic Write Short Packet 1 Parameters

Generic Write Short Packet 2 Parameter

Maximum Read Packet Configuration

Generic Long Write Packet

DCS Write Short Packet 0 Parameter

DCS Write Short Packet 1 Parameter

DCS Write Short Packet 0 Parameter

DCS Write Long Packet

A set of bits in the CMD_PKT_STATUS register report the status of the FIFOs associated with APB interface support.

Generic interface packets are always transported using one of the DSI transmission modes; Video mode or Command mode. If neither of these mode are selected, the packets are not transmitted through the link and the released FIFOs eventually get overflowed.

The transfer of packets through the APB bus is based on the following conditions:

The APB protocol defines that the write and read procedure takes two clock cycles each to be executed. This means that the maximum input data rate through the APB interfaces is always half the speed of the APB clock.

The data input bus has a maximum width of 32 bits. This allows for a relation to be defined between the input APB clock frequency and maximum bit rate achievable by the APB interface.

The DSI link bit rate when using solely APB is equal to (APB clock frequency) * 16 Mbps.

The bandwidth is dependent on the APB clock frequency; the available bandwidth increases with the clock frequency.

To drive the APB interface to achieve high bandwidth Command mode traffic transported by the DSI link, the MIPI Controller should operate in the Command mode only and the APB interface should be the only data source that is currently in use. Thus, the APB interface has the entire bandwidth of the DSI link and does

not share it with any another input interface source.

The memory write commands require maximum throughput from the APB interface, because they contain the most amount of data conveyed by the DSI link. While writing the packet information, first write the payload of a given packet into the payload FIFO using the GEN_PLD_DATA register. When the payload data is for the command parameters, place the first byte to be transmitted in the least significant byte position of the APB data bus.

After writing the payload, write the packet header into the command FIFO. For more information and it should follow the pixel to byte conversion organization referred in the Annexure A of the DCS specification. The follow figures show how the pixel data should be organized in the APB data write bus. The memory write commands are conveyed in DCS long packets. DCS long packets are encapsulated in a DSI packet. The DSI included in the diagrams. In the follow figures, the Write Memory Command can be replaced by the DCS command Write Memory Start and Write Memory Continue.

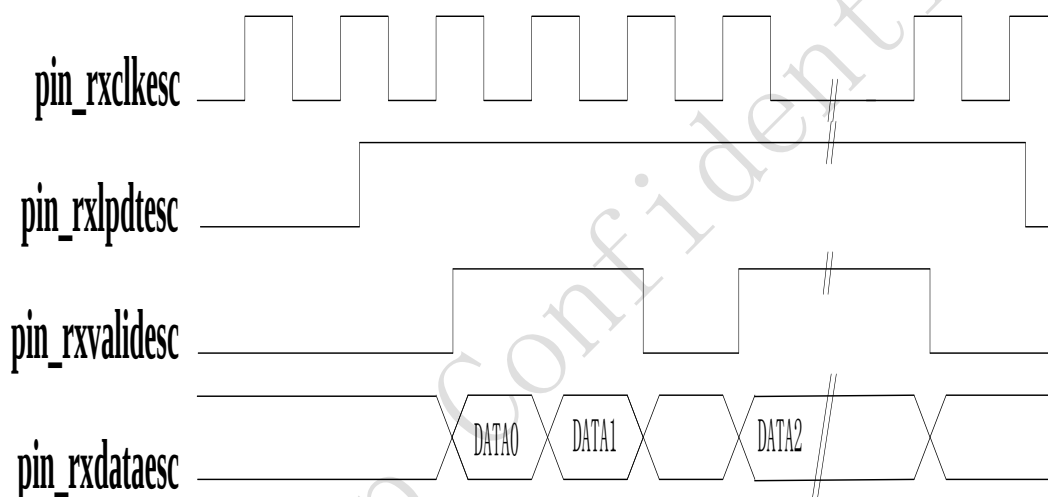


Fig. 7-224 bpp APB Pixel to Byte Organization

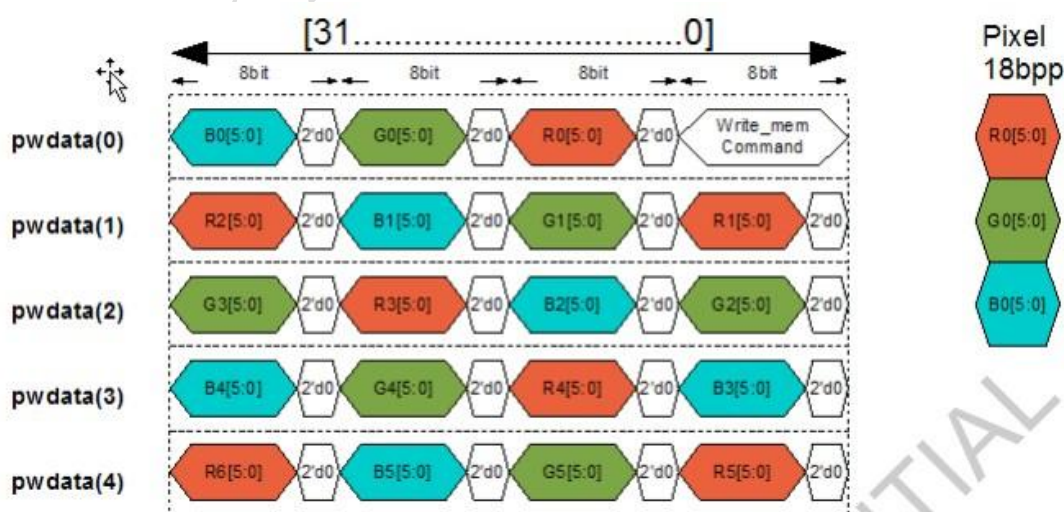


Fig. 7-318 bpp APB Pixel to Byte Organization

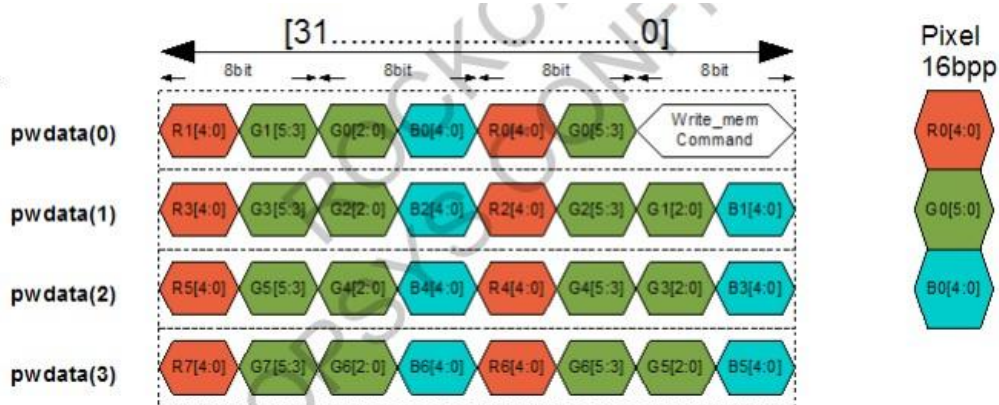


Fig. 7-416 bpp APB Pixel to Byte Organization

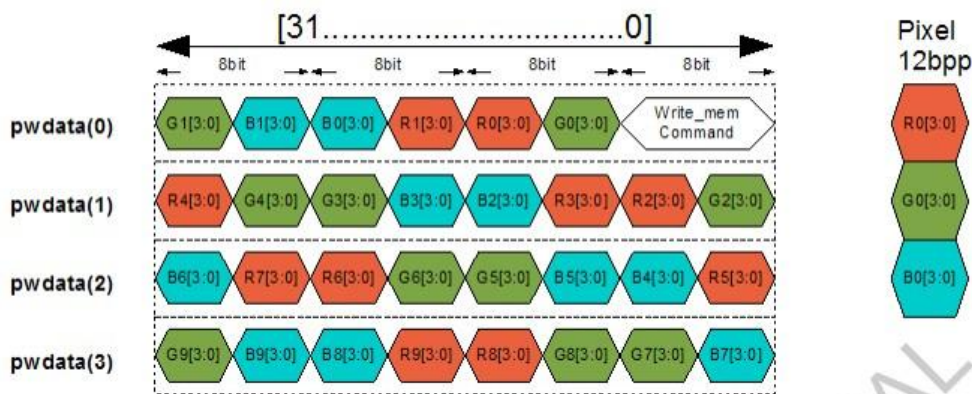


Fig. 7-512 bpp APB Pixel to Byte Organization

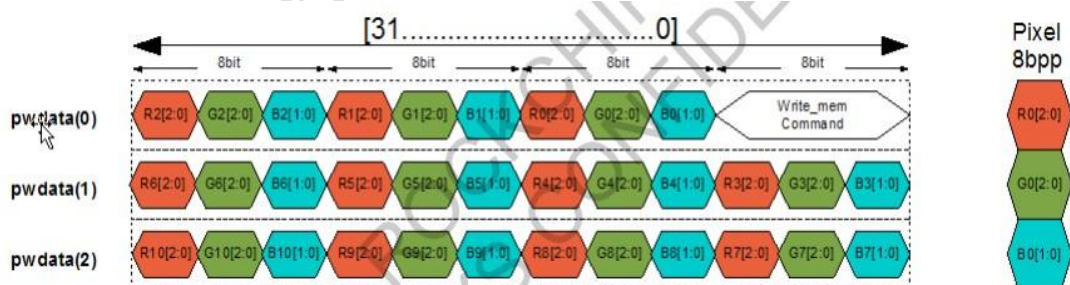


Fig. 7-68 bpp APB Pixel to Byte Organization

7.3.3 .Transmission of Commands in Video Mode

The MIPI Controller supports the transmission of commands, both in high-speed and low-power, while in Video mode. The DSI controller uses Blanking or Low-Power(BLLP) periods to transmit commands inserted through the APB Generic interface. Those periods correspond to the shaded areas of the following figure.

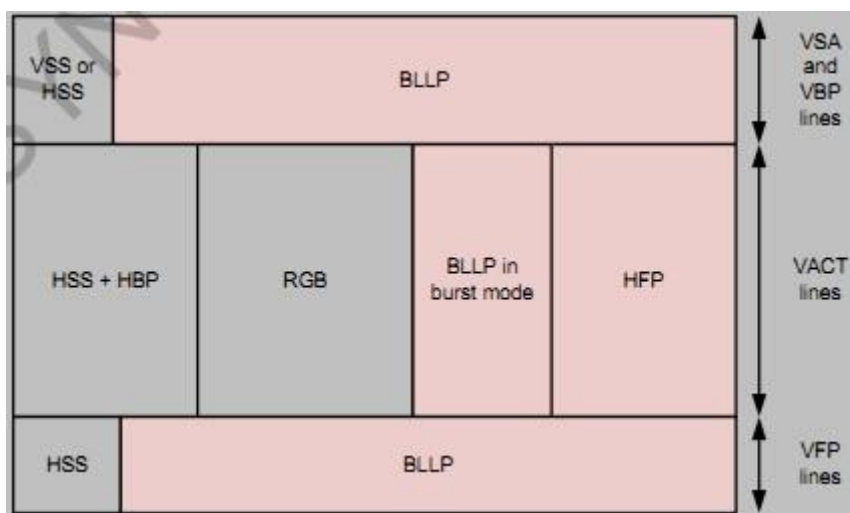


Fig. 7-7 Command Transmission Periods within the Image Area

Commands are transmitted in the blanking periods after the following packet/states:

- Vertical Sync Start (VSS) packets, if the Video Sync pulses are not enabled
- Horizontal Sync End (HSE) packets, in the VSA, VBP, and VFP regions
- Horizontal Sync Start (HSS) packets, if the Video Sync pulses are not enabled in the VSA, VBP, and VFP regions
- Horizontal Active (HACT) state

Only one command is transmitted per line, even in the case of the last line of a frame but one command is possible for each line.

The MIPI Controller avoids sending commands in the last line because it is possible that the last line is shorter than the other ones. For instance, the line time (tL) could be half a cycle longer than the tL on the DPI interface, that is, each line in the frame taking half a cycle from time for the last line. This results in the last line being $(1/2 \text{ cycle}) * (\text{number of lines} - 1)$ shorter than tL.

The dpicolorm and dpishutdn input signals are also able to trigger the sending of command packets. The commands are DSI data types Color Mode On, Color Mode Off, Shut Down Peripheral, and Turn on Peripheral. These commands are not sent in the VACT region. If the lpcmden bit of the VID_MODE_CFG register is 1, these commands are sent in LP mode. In LP mode, the outvact_lpcmd_time field of the LP_CMD_TIM register is used to determine if these commands can be transmitted. It is assumed that outvact_lpcmd_time is greater than or equal to 4 bytes (number of bytes in a short packet), because the DWC_mipi_dsi_host does not transmit these commands on the last line.

If the frame_BTA_ack field is set in the VID_MODE_CFG register, a BTA is generated by DWC_mipi_dsi_host after the last line of a frame. This may coincide with a write command or a read command. In either case, the edpiphalt signal is held asserted until an acknowledge has been received (control of the DSI bus is returned to the host).

If the lpcmden bit of the VID_MODE_CFG register is set to 1, the commands are sent in low-power in Video mode. In this case, it is necessary to calculate the time available, in bytes, to transmit a command in LP mode for Horizontal Front

Porch (HFP), Vertical Sync Active (VSA), Vertical Back Porch (VBP), and Vertical Front Porch(VFP) regions.

The outvact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmit a command in LP mode, based on the escape clock, on a line during the VSA, VBP, and the VFP

$$\text{Outvact_lpcmd_time} = (\text{tL} - (\text{Time to transmit HSS and HSE frames} + \text{tHSA} + \text{Time to enter and leave LP mode} + \text{Time to send the D-PHY LPDT command})) / \text{escape clock period} / 8 / 2$$

Where,

tL=Line time

tHSA=Time to send a short packet (for sync events) or time of the HAS pulse (for sync pulses)

In the above equation, division by eight is done to convert the time available to bytes and division by two is done because one bit is transmitted once in every two escape clock cycles.

The outvact_lpcmd_time filed can be compared directly with the size of the command to be transmitted to determine if there is enough time to transmit the command. The maximum size of a command that can be transmitted in LP mode is limited to 255 bytes by this field. This register must be programmed to a value greater than or equal to 4 bytes for the transmission of the DCTRL commands such as shutdown and colorm in LP mode.

Consider an example with 12.6 μs per line and assume an escape clock frequency of 15 MHz. In this case, 189 escape clock cycles are available to enter and exit LP mode and transmit command. The following are assumed: Sync pulses are not being transmitted)

Two lane byte clock ticks are required to transmit a short packet

phy_lp2hs_time=16

phy_lp2p_time=20

In this example, a 11-byte command can be transmitted as follows:

$$\text{outvact_lpcmd_time} = (12.6\mu\text{s} - (2*10\text{ ns}) - (16*10\text{ ns}) - (20*10\text{ ns}) - (8*66\text{ ns})) / 66\text{ ns} / 8 / 2 = 11\text{ bytes}$$

The invact_lpcmd_time field of the LP_CMD_TIM register indicates the time available (in bytes) to transmute a command in LP mode (based on the escape clock) in the Vertical Active (VACT) region. This time is calculated as follows:

$$\text{Invact_lpcmd_time} = ((\text{tHFP} - \text{Time to enter and leave low-power mode} + \text{Blanking period before the HFP when in Burst mode} - \text{Time to send the D-PHY LPDT command}) / \text{escape clock period}) / 8$$

Where,

tHFP=line time-tHSA-tHBP-tHACT

tHACT=vid_pkt_size*bits_per_pixel*lane_byte_clock_period / num_lanes

The invact_lpcmd_time field can be compared directly with the size of the command to be transmitted to determined if there is time to transmit the command.

Consider an example where the refresh rate is 60 Hz. The number of lines is 1320 (typical). The tL in this case is 12.6 μs . With a lane byte clock of 100 MHz, 1260 clock ticks are available to transmit a single frame. If 800 ticks are used for pixel data then 460 ticks (4.6 μs) are available for Horizontal Sync Start (HSS), HFP, and HBP. Assuming that 2.3 μs is available for HFP and the escape clock is 15MHz, only 34 LP clock ticks are available to enter LP, transmit a command, and return from LP mode. Approximately 12 escape clock ticks are required to

enter and leave LP mode. Therefore, only 1 byte could be transmitted in this period.

A short packet (for example, generic short write) requires a minimum of 4 bytes. Therefore, in this example, commands are not sent in the VACT region. If Burst mode is enabled, more time is available to transmit commands in the VACT region. The following are assumed:

The controller is not in Burst mode

phy_lp2hs_time=16

phy_lp2hs_time=16

In this example, invact_lpcmd_time is calculated as follows:

Invact_lpcmd_time = $(2.3\mu s - (16 \times 10\text{ ns}) - (20 \times 10\text{ ns}) - (8 \times 66\text{ ns})) / 66\text{ ns} / 8 = 2$ bytes

The outvact_lpcmd_time and invact_lpcmd_time fields allow a simple comparison to determine if a command can be transmitted in any of the BLLP periods.

Figure 5-21 illustrates the meaning of invact_lpcmd_time and outvact_lpcmd_time, matching them with the shaded areas and the VACT region.

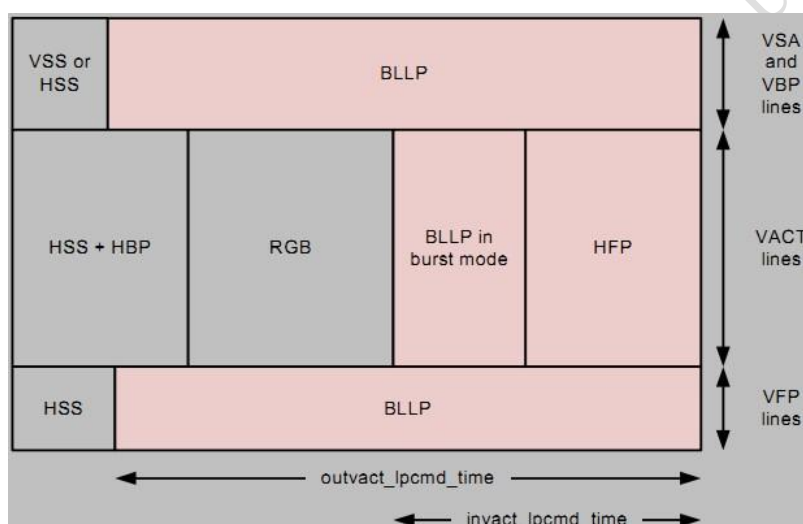


Fig. 7-8 Location of outvact_lpcmd_time and invact_lpcmd_time in the Image Area

If the lpcmden bit of the VID_MODE_CFG register is 0, the commands are sent in high_speed in Video Mode. In this case, the DWC_mipi_dsi_host automatically determines the area where each command can be sent and no programming or calculation is required.

On read command Transmission, the max_rd_time field of the PHY_TMR_CFG register configures the maximum amount of time required to perform a read command in lane byte clock cycles.

The maximum time required to perform a read command in Lane byte clock cycles (max_rd_time) = Time to transmit the read command in LP mode + Time to enter and leave LP mode + Time to return the read data packet from the peripheral device.

The time to return the read data packet from the peripheral depends on the number of bytes read and the escape clock frequency of the peripheral; not the escape clock of the host. The max_rd_time field is used in both HS and LP mode to determine if there is time to complete a read command in a BLLP period.

In high-speed mode (lpcmden=0), max_rd_time is calculated as follows:

max_rd_time = phy_hs2lp_time + Time to return the read data packet from the

peripheral device + phy_hs2hs_time

In low-power mode (lpcmden = 1), max_rd_time is calculated as follows:

max_rd_time = phy_hs2lp_time + LPDT command time + Read command time in LP mode + Time to return the data read from the peripheral device + phy_lp2hs_time

Where,

LPDT command time = $(8 * \text{Host escape clock period}) / \text{Lane byte clock period}$

Read command time in LP mode = $(32 * \text{host escape clock period}) / \text{lane byte clock period}$

It is recommended to keep the maximum number of bytes read from the peripheral to a minimum to have sufficient time available to issue the read commands on a line. Ensure that max_rd_time * Lane byte clock period is less than outvact_lpcmd_time * 8 * Escape clock period of the host.

Otherwise, the read commands are serviced on the last line of a frame and the edpiahalt signal may be asserted. If it is necessary to read a large number of parameters (>16), increase the max_rd_time while the read command is being executed. When the read has completed, decrease the max_rd_time to a lower value.

7.4 Register Description

This section describes the control/status registers of the design.

7.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
MIPIC_VERSION	0x0000	W	0x3131302a	Version of the mipi controller
MIPIC_PWR_UP	0x0004	W	0x00000000	Core power-up
MIPIC_CLKMGR_CFG	0x0008	W	0x00000000	Configuration of the internal clock dividers
MIPIC_DPI_CFG	0x000c	W	0x00000000	The DPI interface configuration.
MIPIC_RESERVED	0x0010	W	0x00000000	Reserved
MIPIC_RESERVED1	0x0014	W	0x00000000	Reserved
MIPIC_PCKHDL_CFG	0x0018	W	0x00000000	Packet handler configuration
MIPIC_VID_MODE_CFG	0x001c	W	0x00000000	Video mode configuration.
MIPIC_VID_PKT_CFG	0x0020	W	0x00000000	Video packet configuration
MIPIC_CMD_MODE_CFG	0x0024	W	0x00000000	Command mode configuration
MIPIC_TMR_LINE_CFG	0x0028	W	0x00000000	Line timing configuration.
MIPIC_VTIMING_CFG	0x002c	W	0x00000000	Vertical timing configuration.
MIPIC_PHY_TMR_CFG	0x0030	W	0x00000000	D-PHY timing configuration
MIPIC_GEN_HDR	0x0034	W	0x00000000	Generic packet header configuration.
MIPIC_GEN_PLD_DATA	0x0038	W	0x00000000	Generic payload data in and out.
MIPIC_CMD_PKT_STATUS	0x003c	W	0x00000000	Command packet status
MIPIC_TO_CNT_CFG	0x0040	W	0x00000000	Timeout timers configuration
MIPIC_ERROR_ST0	0x0044	W	0x00000000	Interrupt status register 0
MIPIC_ERROR_ST1	0x0048	W	0x00000000	Interrupt status register 1
MIPIC_MSK0	0x004c	W	0x00000000	Masks the interrupt generation triggerd by the ERROR_ST0 reg
MIPIC_MSK1	0x0050	W	0x00000000	Masks the interrupt generation triggerd by the ERROR_ST1 reg
MIPIC_PHY_RSTZ	0x0054	W	0x00000000	D-PHY reset control
MIPIC_PHY_IF_CFG	0x0058	W	0x00000000	D-PHY interface configuration
MIPIC_PHY_IF_CTRL	0x005c	W	0x00000000	D-PHY PPI interface control
MIPIC_PHY_STATUS	0x0060	W	0x00000000	D-PHY PPI status interface
MIPIC_RESERVED2	0x0064	W	0x00000000	Reserved
MIPIC_RESERVED3	0x0068	W	0x00000000	Reserved
MIPIC_RESERVED4	0x006c	W	0x00000000	Reserved
MIPIC_LP_CMD_TIM	0x0070	W	0x00000000	Low-power Command Timing Configuration Register.

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

7.4.2 Detail Register Description

MIPIC_VERSION

Address: Operational Base + offset (0x0000)

Version of the mipi controller

Bit	Attr	Reset Value	Description
31:0	RO	0x3131302a	version indicates the version of the mipi_controller

MIPIC_PWR_UP

Address: Operational Base + offset (0x0004)

Core power-up

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	shutdownz This bit indicates the core power-up or the reset 0-Reset 1-Power-up

MIPIC_CLKMGR_CFG

Address: Operational Base + offset (0x0008)

Configuration of the internal clock dividers

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved
15:8	RW	0x00	TO_CLK_DIVISION This field indicates the division factor for the Time Out clock used as the timing unit in the configuration of HS to LP and LP to HS transition error.
7:0	RW	0x00	TX_ESC_CLK_DIVISION Field0000 Abstract This field indicates the division factor for the TX_Escape clock source(lanebyteclk).The value 0 and 1 stop the TX_ESC clock generation

MIPIC_DPI_CFG

Address: Operational Base + offset (0x000c)

The DPI interface configuration.

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	en18_loosely Field0000 Abstract When set to 1,this bit enables 18 loosely packed pixel stream.
9	RW	0x0	colorm_active_low When set to 1,this bit configures the color mode pin as active low

Bit	Attr	Reset Value	Description
8	RW	0x0	shutd_active_low When set to 1,this bit configures the shut down pin as active low
7	RW	0x0	hsync_active_low When set to 1,this bit configures the horizontal synchronism pin as active low.
6	RW	0x0	vsync_active_low When set to 1,this bit configures the vertical synchronism pin as active low
5	RW	0x0	dataen_active_low When set to 1,this bit configures the data enable pin as active low
4:2	RW	0x0	dpi_color_coding This field configures the DPI color coding as follows: 000:16bit configuration 1 001:16bit configuration 2 010:16bit configuration 3 011:18bit configuration 1 100:18bit configuration 2 101,110,and 111:24bits
1:0	RW	0x0	dpi_vid This field configures the DPI virtual channel id that is indexed to the Video mode packets.

MIPIC_RESERVED

Address: Operational Base + offset (0x0010)

Reserved

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Reserved

MIPIC_RESERVED1

Address: Operational Base + offset (0x0014)

Reserved

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Reserved Reserved1

MIPIC_PCKHDL_CFG

Address: Operational Base + offset (0x0018)

Packet handler configuration

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:5	RW	0x0	gen_vid_rx This field indicates the Generic interface read-back virtual channel identification
4	RW	0x0	en_CRC_rx When set to 1, this bit enables the CRC reception and error reporting
3	RW	0x0	en_ECC_rx When set to 1, this bit enables the ECC reception, error correction, and reporting
2	RW	0x0	en_BTA When set to 1, this bit enables the Bus Turn-Around(BTA) request.
1	RW	0x0	en_EOTp_rx Field0000 Abstract When set to 1, this bit enables the EOTp reception
0	RW	0x0	en_EOTp_tx Field0000 Abstract When set to 1, this bit enables the EOTp transmission

MIPIC_VID_MODE_CFG

Address: Operational Base + offset (0x001c)

Video mode configuration.

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RW	0x0	lpcmden When set to 1, this bit enables the command transmission only in low-power mode
11	RW	0x0	frame_BTA_ack When set to 1, this bit enables the request for an acknowledge response at the end of a frame
10	RW	0x0	en_null_pkt When set to 1, this bit enables the transmission of null packets in the HACT period.
9	RW	0x0	en_multi_pkt When set to 1, this bit enables the transmission of multi video packets in the HACT period

Bit	Attr	Reset Value	Description
8	RW	0x0	en_lp_hfp When set to 1,this bit enables the return to low-power inside the HFP period when timing allows.
7	RW	0x0	en_lp_hbp When set to 1,this bit enables the return to low-power inside the HBP period when timing allows.
6	RW	0x0	en_lp_vact When set to 1,this bit enables the return to low-power inside the VACT period when timing allows.
5	RW	0x0	en_lp_vfp When set to 1,this bit enables the return to low-power inside the VFP period when timing allows.
4	RW	0x0	en_lp_vbp When set to 1,this bit enables the return to low-power inside the VBP period when timing allows.
3	RW	0x0	en_lp_vsa When set to 1,this bit enables the return to low-power inside the VSA period when timing allows.
2:1	RW	0x0	vid_mode_type This field indicates the video mode transmission type as follows: 00:Non-burst with sync pulses 01:Non-burst with sync events 10 and 11:Burst with sync pulses
0	RW	0x0	en_video_mode When set to 1,this bit enables the DPI Video mode transmission.

MIPI_CVID_PKT_CFG

Address: Operational Base + offset (0x0020)

Video packet configuration

Bit	Attr	Reset Value	Description
31	RO	0x0	reserved
30:21	RW	0x000	null_pkt_size This field configures the number of bytes in a null packet
20:11	RW	0x000	num_chunks This field configures the number of chunks to be transmitted during a line period(a chunk is a video packet or a null packet)

Bit	Attr	Reset Value	Description
10:0	RW	0x000	vid_pkt_size This field configures the number of pixels on a single video packet. if you use the 18-bit mode and do not enable loosely packed stream, this value must be a multiple of 4.

MIPI_CMD_MODE_CFG

Address: Operational Base + offset (0x0024)

Command mode configuration

Bit	Attr	Reset Value	Description
31:11	RO	0x0	reserved
10	RW	0x0	max_rd_pkt_size This bit configures the maximum read packet size command transmission type: 0:High-speed 1:Low-power
9	RW	0x0	dcs_sr_0p_tx This bit configures the DCS short read packet with zero parameter command transmission type: 0:High-speed 1:Low-power
8	RW	0x0	dcs_sw_1p_tx This bit configures the DCS short write packet with one parameter command transmission type: 0:High-speed 1:Low-power
7	RW	0x0	dcs_sw_0p_tx This bit configures the DCS short write packet with zero parameter command transmission type: 0:High-speed 1:Low-power
6	RW	0x0	gen_sr_2p_tx This bit configures the Generic short read packet with two parameter command transmission type: 0:High-speed 1:Low-power
5	RW	0x0	gen_sr_1p_tx This bit configures the Generic short read packet with one parameter command transmission type: 0:High-speed 1:Low-power

Bit	Attr	Reset Value	Description
4	RW	0x0	gen_sr_0p_tx This bit configures the Generic short read packet with zero parameter command transmission type: 0:High-speed 1:Low-power
3	RW	0x0	gen_sw_2p_tx This bit configures the Generic short write packet with two parameter command transmission type: 0:High-speed 1:Low-power
2	RW	0x0	gen_sw_1p_tx This bit configures the Generic short write packet with one parameter command transmission type: 0:High-speed 1:Low-power
1	RW	0x0	gen_sw_0p_tx This bit configures the Generic short write packet with zero parameter command transmission type: 0:High-speed 1:Low-power
0	RW	0x0	en_cmd_mode When set to 1,this bit enables the Command mode protocol for transmissions

MIPIC_TMR_LINE_CFG

Address: Operational Base + offset (0x0028)

Line timing configuration.

Bit	Attr	Reset Value	Description
31:18	RW	0x0000	hline_time This field configures the size of the total lines counted in lane byte cycles.
17:9	RW	0x000	hbp_time This field configures the Horizontal Back Porch period in lane byte clock cycles
8:0	RW	0x000	hsa_time This field configures the Horizontal Synchronism Active period in lane byte clock cycles.

MIPIC_VTIMING_CFG

Address: Operational Base + offset (0x002c)

Vertical timing configuration.

Bit	Attr	Reset Value	Description
31:27	RO	0x0	reserved
26:16	RW	0x000	v_active_lines This field configures the Vertical Active period measured in horizontal lines.
15:10	RW	0x00	vfp_lines This field configures the Vertical Front Porch period measured in horizontal lines.
9:4	RW	0x00	vbp_lines This field configures the Vertical Back Porch period measured in horizontal lines.
3:0	RW	0x0	vsa_line This field configures the Vertical Synchronism Active period measured in horizontal lines.

MIPIC_PHY_TMR_CFG

Address: Operational Base + offset (0x0030)

D-PHY timing configuration

Bit	Attr	Reset Value	Description
31:24	RW	0x00	phy_hs2lp_time This field configures the maximum time that the PHY takes to go from high-speed to low-power transmission measured in lane byte clock cycles.
23:16	RW	0x00	phy_lp2hs_time This field configures the maximum time that the PHY takes to go from low-power to high-speed transmission measured in lane byte clock cycles.
15	RW	0x0	reserved reserved for future use
14:0	RW	0x0000	max_rd_time This field configures the maximum time required to perform a read command in lane byte clock cycles. This register can only be modified when read commands are not in progress.

MIPIC_GEN_HDR

Address: Operational Base + offset (0x0034)

Generic packet header configuration.

Bit	Attr	Reset Value	Description
31:24	RO	0x0	reserved

Bit	Attr	Reset Value	Description
23:16	RW	0x00	gen_WC_MSbyte This field configures the most significant byte of the header packet's Word count for long packets or data 1 for short packets.
15:8	RW	0x00	gen_WC_LSbyte This field configures the least significant byte of the header packet's Word count for long packets or data 0 for short packets.
7:6	RW	0x0	gen_VC This field configures the virtual channel id of the header packet.
5:0	RW	0x00	gen_DT This field configures the packet data type of the header packet

MIPIC_GEN_PLD_DATA

Address: Operational Base + offset (0x0038)

Generic payload data in and out.

Bit	Attr	Reset Value	Description
31:24	RW	0x00	gen_pld_b4 This field indicates byte 4 of the packet payload.
23:16	RW	0x00	gen_pld_b3 This field indicates byte 3 of the packet payload.
15:8	RW	0x00	gen_pld_b2 This field indicates byte 2 of the packet payload.
7:0	RW	0x00	gen_pld_b1 This field indicates byte 1 of the packet payload.

MIPIC_CMD_PKT_STATUS

Address: Operational Base + offset (0x003c)

Command packet status

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	reserved reserved
6	RW	0x0	gen_rd_cmd_busy This bit is set when a read command is issued and cleared when the entire response is stored in the FIFO

Bit	Attr	Reset Value	Description
5	RW	0x0	gen_pld_r_full This bit indicates the full status of the generic read payload FIFO Vaule after reset:0x0
4	RO	0x0	gen_pld_r_empty This bit indicates the empty status of the generic read payload FIFO Vaule after reset:0x1
3	RO	0x0	gen_pld_w_full This bit indicates the full status of the generic write payload FIFO Vaule after reset:0x0
2	RO	0x0	gen_pld_w_empty This bit indicates the empty status of the generic write payload FIFO Vaule after reset:0x1
1	RO	0x0	gen_cmd_full This bit indicates the full status of the generic command FIFO Vaule after reset:0x0
0	RO	0x0	gen_cmd_empty This bit indicates the empty status of the generic command FIFO Vaule after reset:0x1

MIPIC_TO_CNT_CFG

Address: Operational Base + offset (0x0040)

Timeout timers configuration

Bit	Attr	Reset Value	Description
31:16	RW	0x0000	lprx_to_cnt This field configures the timeout counter that triggers a low-power reception timeout contention detection(measured in TO_CLK_DIVISION cycles)
15:0	RW	0x0000	hstx_to_cnt This field configures the timeout counter that triggers a high-speed transmission timeout contention detection(measured in TO_CLK_DIVISION cycles)

MIPIC_ERROR_ST0

Address: Operational Base + offset (0x0044)

Interrupt status register 0

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved
20	RO	0x0	dphy_errors_4 This bit indicates LP1 contention error ErrContentionLP1 from Lane 0
19	RO	0x0	dphy_errors_3 This bit indicates LP0 contention error ErrContentionLP0 from Lane 0
18	RO	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0
17	RO	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RO	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RO	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Display Acknowledge error report
14	RO	0x0	ack_with_err_14 This bit retrieves the reserved(specific to device) from the Display Acknowledge error report
13	RO	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Display Acknowledge error report
12	RO	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report
11	RO	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Display Acknowledge error report
10	RO	0x0	ack_with_err_10 This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report
9	RO	0x0	ack_with_err_9 This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report
8	RO	0x0	ack_with_err_8 This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report
7	RO	0x0	ack_with_err_7 This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
6	RO	0x0	ack_with_err_6 This bit retrieves the False Control error from the Display Acknowledge error report
5	RO	0x0	ack_with_err_5 This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report
4	RO	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error error from the Display Acknowledge error report
3	RO	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report
2	RO	0x0	ack_with_err_2 This bit retrieves the EoT sync error from the Display Acknowledge error report
1	RO	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Display Acknowledge error report
0	RO	0x0	ack_with_err_0 This bit retrieves the SoT error from the Display Acknowledge error report

MIPIC_ERROR_ST1

Address: Operational Base + offset (0x0048)

Interrupt status register 1

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_rcv_err This bit indicates that during a generic interface packet read back,the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data,the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build,the payload FIFO becomes empty and corrupt data is sent.

Bit	Attr	Reset Value	Description
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the command is not written.
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eopt_err This bit indicates that the EOTp packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in a received packet.
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected and corrected in a received packet.
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected.
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected.

MIPIC_MSK0

Address: Operational Base + offset (0x004c)

Masks the interrupt generation triggered by the ERROR_ST0 reg

Bit	Attr	Reset Value	Description
31:21	RO	0x0	reserved

Bit	Attr	Reset Value	Description
20	RW	0x0	dphy_errors_4 This bit indicates LP1 contention error ErrContentionLP1 from Lane 0
19	RW	0x0	dphy_errors_3 This bit indicates LP0 contention error ErrContentionLP0 from Lane 0
18	RW	0x0	dphy_errors_2 This bit indicates control error ErrControl from Lane 0
17	RW	0x0	dphy_errors_1 This bit indicates ErrSyncEsc low-power data transmission synchronization error from Lane 0
16	RW	0x0	dphy_errors_0 This bit indicates ErrEsc escape entry error from Lane 0
15	RW	0x0	ack_with_err_15 This bit retrieves the DSI protocol violation from the Display Acknowledge error report
14	RW	0x0	ack_with_err_14 This bit retrieves the reserved(specific to device) from the Display Acknowledge error report
13	RW	0x0	ack_with_err_13 This bit retrieves the invalid transmission length from the Display Acknowledge error report
12	RW	0x0	ack_with_err_12 This bit retrieves the DSI VC ID Invalid from the Display Acknowledge error report
11	RW	0x0	ack_with_err_11 This bit retrieves the not recognized DSI data type from the Display Acknowledge error report
10	RW	0x0	ack_with_err_10 This bit retrieves the checksum error(long packet only) from the Display Acknowledge error report
9	RW	0x0	ack_with_err_9 This bit retrieves the ECC error,multi-bit(detected and corrected) from the Display Acknowledge error report
8	RW	0x0	ack_with_err_8 This bit retrieves the ECC error,single-bit(detected and corrected) from the Display Acknowledge error report
7	RW	0x0	ack_with_err_7 This bit retrieves the reserved(specific to device) error from the Display Acknowledge error report

Bit	Attr	Reset Value	Description
6	RW	0x0	ack_with_err_6 This bit retrieves the False Control error from the Display Acknowledge error report
5	RW	0x0	ack_with_err_5 This bit retrieves the HS Receive Timeout error from the Display Acknowledge error report
4	RW	0x0	ack_with_err_4 This bit retrieves the LP Transmit Sync error error from the Display Acknowledge error report
3	RW	0x0	ack_with_err_3 This bit retrieves the Escape Mode Entry command error from the Display Acknowledge error report
2	RW	0x0	ack_with_err_2 This bit retrieves the EoT sync error from the Display Acknowledge error report
1	RW	0x0	ack_with_err_1 This bit retrieves the SoT Sync error from the Display Acknowledge error report
0	RW	0x0	ack_with_err_0 This bit retrieves the SoT error from the Display Acknowledge error report

MIPIC_MSK1

Address: Operational Base + offset (0x0050)

Masks the interrupt generation triggered by the ERROR_ST1 reg

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	gen_pld_rcv_err This bit indicates that during a generic interface packet read back, the payload FIFO becomes full and the received data is corrupted.
11	RO	0x0	gen_pld_rd_err This bit indicates that during a DCS read data, the payload FIFO becomes empty and the data sent to the interface is corrupted
10	RO	0x0	gen_pld_send_err This bit indicates that during a Generic interface packet build, the payload FIFO becomes empty and corrupt data is sent.

Bit	Attr	Reset Value	Description
9	RO	0x0	gen_pld_wr_err This bit indicates that the system tried to write a payload data through the Generic interface and the FIFO is full. Therefore, the command is not written.
8	RO	0x0	gen_cmd_wr_err This bit indicates that the system tried to write a command through the Generic interface and the FIFO is full. Therefore, the command is not written.
7	RO	0x0	dpi_pld_wr_err This bit indicates that during a DPI pixel line storage, the payload FIFO becomes full and the data stored is corrupted.
6	RO	0x0	eopt_err This bit indicates that the EOTp packet is not received at the end of the incoming peripheral transmission.
5	RO	0x0	pkt_size_err This bit indicates that the packet size error is detected during the packet reception.
4	RO	0x0	crc_err This bit indicates that the CRC error is detected in a received packet.
3	RO	0x0	ecc_multi_err This bit indicates that the ECC multiple error is detected and corrected in a received packet.
2	RO	0x0	ecc_single_err This bit indicates that the ECC single error is detected and corrected in a received packet.
1	RO	0x0	to_lp_rx This bit indicates that the low-power reception timeout counter reached the end and contention detection is detected.
0	RO	0x0	to_hs_tx This bit indicates that the high-speed transmission timeout counter reached the end and contention detection is detected.

MIPI_CPHY_RSTZ

Address: Operational Base + offset (0x0054)

D-PHY reset control

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	phy_enabledclk When set to 1, this bit enables the D-PHY Clock Lane Module
1	RW	0x0	reserved1 reserved
0	RW	0x0	reserved reserved

MIPIC_PHY_IF_CFG

Address: Operational Base + offset (0x0058)

D-PHY interface configuration

Bit	Attr	Reset Value	Description
31:10	RO	0x0	reserved
9:2	RW	0x00	phy_stop_wait_time This field configures the minimum wait period to request a high-speed transmission after the Stop state is accounted in clock lane cycles.
1:0	RW	0x0	n_lanes This field configures the number of active data lanes: 00: One data lane (lane 0) 01: Two data lanes (lanes 0 and 1) 10: Three data lanes (lanes 0, 1, and 2) 11: Four data lanes (lanes 0, 1, 2, and 3)

MIPIC_PHY_IF_CTRL

Address: Operational Base + offset (0x005c)

D-PHY PPI interface control

Bit	Attr	Reset Value	Description
31:9	RO	0x0	reserved
8:5	RW	0x0	phy_tx_triggers This field controls the trigger transmissions.
4	RW	0x0	phy_txexitulpslan ULPS mode Exit on all active data lanes
3	RW	0x0	phy_txrequlpslan ULPS mode Request on all active data lanes
2	RW	0x0	phy_txexitulpsclk ULPS mode Exit on clock lane
1	RW	0x0	phy_txrequlpsclk ULPS mode Request on clock lane
0	RW	0x0	phy_txrequestclkhs This bit controls the D-PHY PPI txrequestclkhs signal

MIPI_CPHY_STATUS

Address: Operational Base + offset (0x0060)

D-PHY PPI status interface

Bit	Attr	Reset Value	Description
31:13	RO	0x0	reserved
12	RO	0x0	ulpsactivenot3lane This bit indicates the status of ulpsactivenot3lane D-PHY signal
11	RO	0x0	phystopstate3lane This bit indicates the status of phystopstate3lane D-PHY signal
10	RO	0x0	ulpsactivenot2lane This bit indicates the status of ulpsactivenot2lane D-PHY signal
9	RO	0x0	phystopstate2lane This bit indicates the status of phystopstate2lane D-PHY signal
8	RO	0x0	ulpsactivenot1lane This bit indicates the status of ulpsactivenot1lane D-PHY signal
7	RO	0x0	phystopstate1lane This bit indicates the status of phystopstate1lane D-PHY signal
6	RW	0x0	rxulpsesc0lane This bit indicates the status of rxulpsesc0lane D-PHY signal
5	RO	0x0	ulpsactivenot0lane This bit indicates the status of ulpsactivenot0lane D-PHY signal
4	RO	0x0	phystopstate0lane This bit indicates the status of phystopstate0lane D-PHY signal
3	RO	0x0	phyulpsactivenotclk This bit indicates the status of phyulpsactivenotclk D-PHY signal
2	RO	0x0	phystopstatecklane This bit indicates the status of phystopstatecklane D-PHY signal
1	RO	0x0	phydirection This bit indicates the status of phydirection D-PHY signal

Bit	Attr	Reset Value	Description
0	RO	0x0	phylock This bit indicates the status of phylock D-PHY signal

MIPIC_RESERVED2

Address: Operational Base + offset (0x0064)

Reserved

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Reserved Reserved

MIPIC_RESERVED3

Address: Operational Base + offset (0x0068)

Reserved

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Reserved Reserved

MIPIC_RESERVED4

Address: Operational Base + offset (0x006c)

Reserved

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x0	Reserved Reserved

MIPIC_LP_CMD_TIM

Address: Operational Base + offset (0x0070)

Low-power Command Timing Configuration Register.

Bit	Attr	Reset Value	Description
31:16	RO	0x0	reserved

Bit	Attr	Reset Value	Description
15:8	RW	0x00	outvact_lpcmd_time outside VACT region command time. This field configures the time available to transmit a command in low-power mode. The time value is expressed in a number of bytes format. The number of bytes represents the maximum size of a packet that can fit in a line during the VSA, VBP, and VFP region. This field must be configured with a value greater than or equal to four bytes to allow the transmission of the DCTRL commands such as shutdown and colorm in low-power mode.
7:0	RW	0x00	invact_lpcmd_time Inside VACT region command time. This field configures the time available to transmit a command in low-power mode. The time value is expressed in a number of bytes format. The number of bytes represents the maximum size of the packet that can fit a line during the VACT region.

7.5 Application Notes

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the Innosilicon D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

Perform the following steps to configure the DPI packet transmission:

Step1: Global configuration:

Configure n_lanes (PHY_IF_CFG-[1:0]) to define the number of lanes in which the controller has to perform high-speed transmissions.

Step2: Configure the DPI Interface to define how the DPI interface interacts with the controller.

Configure dpi_vid (DPI_CFG-[1:0]): This field configures the virtual channel that the packet generated by the DPI interface is indexed to.

Configure dpi_color_coding (DPI_CFG-[4:2]): This field configures the bits per pixels that the interface transmits and also the variant configuration of each bpp. If you select 18 bpp, and the Enable_18_loosely_packed is not active, the number or pixels per line should be a multiple of four.

Configure dataen_active_low (DPI_CFG-[5]): This bit configures the polarity of the dpidataen signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[6]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[7]): This bit configures the polarity of the dpivsync signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[8]): This bit configures the polarity of the dpishutdn signal and enables if it is active low.

Configure vsync_active_low(DPI_CFG-[9]): This bit configures the polarity of the dpicolorm signal and enables if it is active low.

Configure `en_18_loosely` (DPI_CFG-[10]): This bit configures if the pixel packing is done loosely or packed when `dpi_color_coding` is 18 bpp. This bit enables loosely packing.

Step3: Select the Video Transmission Mode to define how the processor requires the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video line to be transported through the DSI link.

Configure low-power transitions (VID_MODE_CFG-[8:3]): This defines the video periods which are permitted to go to low-power if there is available time to do so.

Configure `frame_BTA_ack` (VID_MODE_CFG-[11]): This specifies if the controller should request the peripheral acknowledge message at the end of frames.

Burst mode: In this mode, the entire active pixel line is buffered into a FIFO and transmitted in a single packet with no interruptions. This transmission mode requires that the DPI Pixel FIFO has the capacity to store a full line of active pixel data inside it. This mode is optimally used if the difference between pixel required bandwidth and DSI link bandwidth is very different. This enables the `DWC_mipi_dsi_host` to quickly dispatch the entire active video line in a single burst of data and then return to low-power mode.

Configure the register field `vid_mode_type` (VID_MODE_CFG-[10]), `num_chunks` (VID_PKT_CFG-[20:11]), and `null_pkt_size` (VID_PKT_CFG-[30:21]) are automatically ignored by the `DWC_mipi_dsi_host`.

Non-Burst mode: In this mode, the processor uses the partitioning properties of the `DWC_mipi_dsi_host` to divide the video line transmission into several DSI packets. This is done to match the pixel required bandwidth with the DSI link bandwidth. With this mode, the controller configuration does not require a full line of pixel data to be stored inside the DPI Pixel FIFO. It requires only the content of one video packet.

Configure the `vid_mode_type` field (VID_MODE_CFG-[2:1]) with 2'b0x.

Configure the `vid_mode_type` field (VID_MODE_CFG-[2:1]) with 2'b00x to enable the transmission of sync pulses.

Configure the `vid_mode_type` field (VID_MODE_CFG-[2:1]) with 2'b01x to enable the transmission of sync events.

Configure the `vid_mode_type` field (VID_MODE_CFG-[10:0]) with the number of pixels to be transmitted in a single packet.

Configure the `en_multi_pkt` field (VID_MODE_CFG-[9]) to enable the division of the active video transmission into more than one packet.

Configure the `num_chunks` field (VID_MODE_CFG-[20:11]) with the number of video chunks that the active video transmission is divided into.

Configure the `en_null_pkt` field (VID_MODE_CFG-[10]) to enable the insertion of null packets between video packets.

The field is effective only when `en_multi_pkt` field is activated, otherwise the controller ignores it and does not send the null packets.

Configure the `null_pkt_size` field (VID_PKT_CFG-[30:21]) with the actual size of the inserted null packet.

Step4: Define the DPI Horizontal timing configuration as follows:

Configure the `hline_time` field (TMR_LINE_CFG-[31:18]) with the time taken by a DPI video line accounted in Clock Lane bytes clock cycles (for a clock lane at 500 MHz the Lane byte clock period is 8 ns). When the DPI clock and Clock Lane clock are not multiples, the `hline_time` is a result of a round of a number. If the `DWC_mipi_dsi_host` is configured to go to low-power, it is possible that the error included in a line is incremented with the next one. At the end of several lines,

the DWC_mipi_dsi_host can have a number of errors that can cause a malfunction of the video transmission.

Configure the hsa_time field (TMR_LINE_CFG-[8:0]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns).

Configure the hbp_time field (TMR_LINE_CFG-[17:9]) with the time taken by a DPI Horizontal Sync Active period accounted in Clock Lane byte clock cycles (normally a period of 8ns). Special attention should be given to the calculation of this parameter.

Step5: Define the Vertical line configuration:

Configure the vsa_lines field (VTIMING_CFG-[3:0]) with the number of lines existing in the DPI Vertical Sync Active period.

Configure the vbp_lines field (VTIMING_CFG-[9:4]) with the number of lines existing in the DPI Vertical Back Porch period.

Configure the vfp_lines field (VTIMING_CFG-[15:10]) with the number of lines existing in the DPI Vertical Front Porch period.

Configure the v_active_lines field (VTIMING_CFG-[26:16]) with the number of lines existing in the DPI Vertical Active period.

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Chapter 8 MIPI D-PHY

8.1 Overview

The MIPI D-PHY integrates a MIPI® V1.0 compatible PHY that supports up to 1GHz high speed data receiver, plus a MIPI® low-power low speed transceiver that supports data transfer in the bi-directional mode. It supports the full specifications described in V1.0 of the D-PHY spec. The D-PHY is built in with a standard digital interface to talk to MIPI Host controller. The architecture supports connection of multiple data lanes in parallel – up to 4 data lanes can be connected to increase the total through-put, customizable to user determined configurations. The MIPI D-PHY supports the electrical portion of MIPI D-PHY V1.0 standard, covering all transmission modes (ULP/LP/HS).

The MIPI D-PHY supports the following features:

- Mixed-signal D-PHY mixed-signal hard-macro- LS Transmitter and LS/HS Receiver solution
- Designed to MIPI® v1.0 Specifications
- Integrated PHY Protocol Interface (PPI) supports interface to CSI, DSI and UniPro™ MIPI® protocols
- 1.0GHz maximum data transfer rate per lane
- Expandable to support 4 data lanes, providing up to 4Gbps transfer rate
- HS, LP and ULPS modes supported
- 10Mbps per lane in low-power mode
- Unidirectional and bi-directional modes supported
- Automatic termination control for HS and LP modes
- Low-Power dissipation: HS less than 3mA/Lane
- Tx/Rx Buffers with tunable On-Die-Termination and advanced equalization.
- Embedded ESD, boundary scan support logic.

8.2 Block Diagram

The MIPI D-PHY configuration contains one Clock Lane Module and four Data Lane Modules. Each of these PHY Lane Modules communicates via two Lines to a complementary part at the other side of the Lane Interconnect. The following diagram shows the D-PHY architecture.

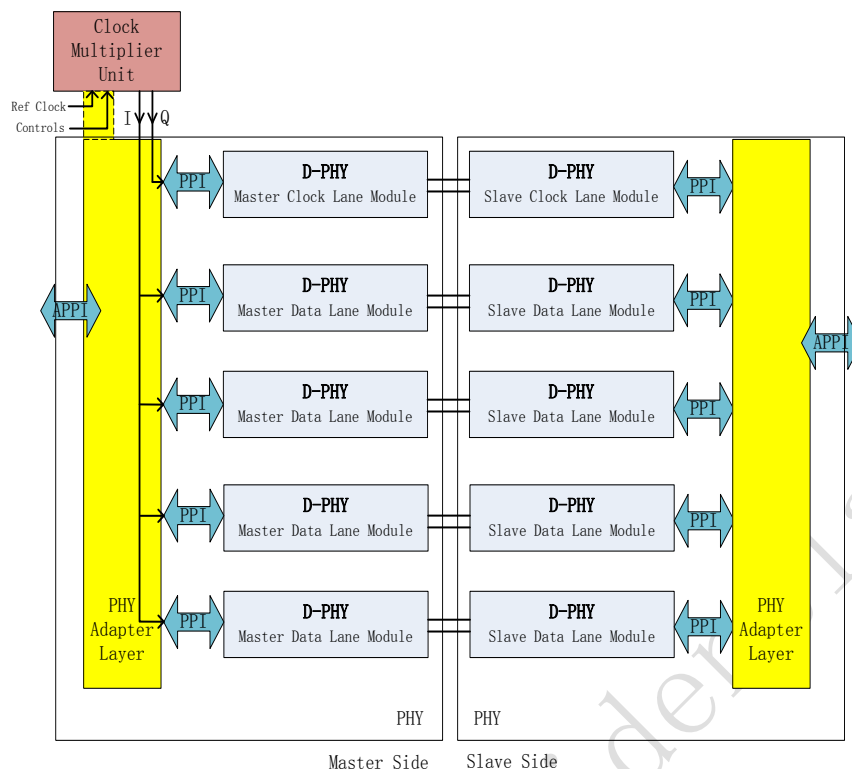


Fig. 8-1 MIPI D-PHY simplified Block diagram with master to slave

The following diagram shows a Universal Lane Module Diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all Lane types. The requirements for the 'Control and Interface Logic' (CIL) function depend on the Lane type and Lane side.

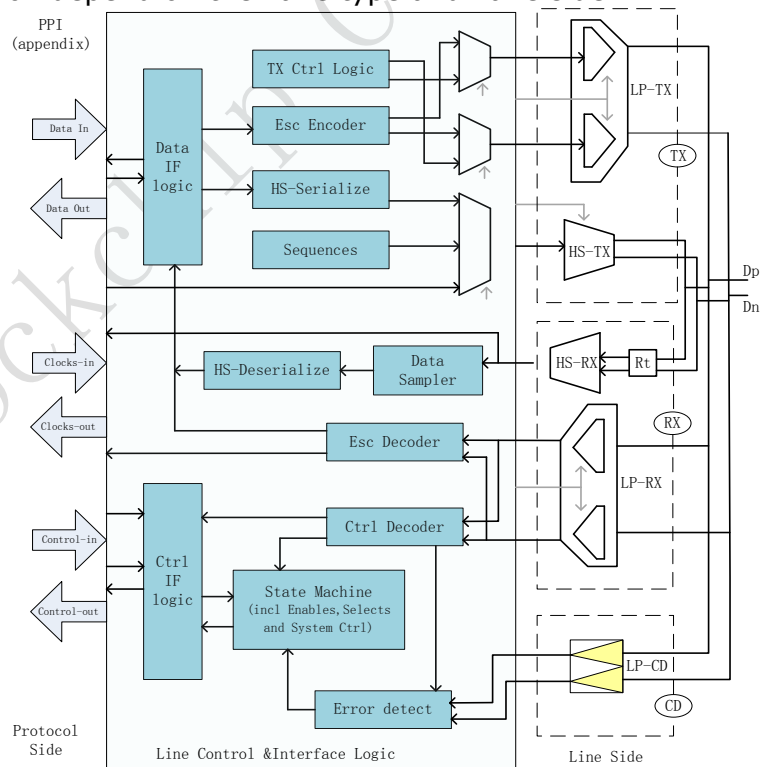


Fig. 8-2MIPI D-PHY V1.0 detailed block diagram

8.3 Function Description

The MIPI D-PHY transceiver is designed to reliably transmit HS and LP/ULP data/clock over the channel and recover the MIPI LP data stream from any MIPI input signal. It consists of 4 data transceiver paths and 1 clock transmitting path. For each data lane a HS transmitter and a LP transceiver is necessary to transmit/recover the data streams, for the clock lane, a HS/LP transmitter is designed to output the high speed clock signal over the channel.

A HS differential signal driven on the Dp and Dn pins is generated by a differential output driver. For reference, Dp is considered as the positive side and Dn as the negative side. High speed current switches are designed to output data streams over the channels.

The Low-Power receiver is an un-terminated, single-ended receiver circuit. LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver can filter out noise pulses and RF interference. Furthermore, any spikes with a pulse width smaller than 20ns will be rejected.

Contention Detector (LP-CD) is designed in Data Lane to monitor the line voltage on each Low-Power signal. The LP-CD is used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than 450mV.

The Low-Power transmitter is a slew-rate controlled push-pull driver. The minimum pull-down and pull-up impedance of LP driver is 110 ohm. At the same time tunable slew rate control logic is available for eye pattern requirement.

8.4 Register Description

This section describes the control/status registers of the design. While you are reading this chapter please note that the offset address[7:0] is distributed two parts, one from the bit7 to bit5 is the first address, the other from the bit4 to bit0 is the second address. When you configure the registers, you must set both of them. The Clock Lane and Data Lane use the same registers with the same second address, but the first address is different. Its apb base address is 0xc00.

8.4.1 Register Summary

Name	Offset	Size	Reset Value	Description
MIIPHY_MIIPHY_REG0	0x0000	W	0x00000001	mipi phy register 0
MIIPHY_MIIPHY_REG1	0x0004	W	0x00000003	mipi phy register 1
MIIPHY_MIIPHY_REG3	0x000c	W	0x00000003	mipi phy register 3
MIIPHY_MIIPHY_REG4	0x0010	W	0x0000007d	mipi phy register 4
MIIPHY_MIIPHY_REG20	0x0080	W	0x00000001	mipi phy register 20
MIIPHY_MIIPHY_REG40	0x0100	W	0x0000000b	mipi phy register 40
MIIPHY_MIIPHY_REG45	0x0114	W	0x00000005	mipi phy register 45
MIIPHY_MIIPHY_REG46	0x0118	W	0x00000000	mipi phy register 46
MIIPHY_MIIPHY_REG47	0x011c	W	0x00000000	mipi phy register 47
MIIPHY_MIIPHY_REG48	0x0120	W	0x00000000	mipi phy register 48
MIIPHY_MIIPHY_REG49	0x0124	W	0x00000000	mipi phy register 49
MIIPHY_MIIPHY_REG4A	0x0128	W	0x00000000	mipi phy register 4a
MIIPHY_MIIPHY_REG4B	0x012c	W	0x00000000	mipi phy register 4b
MIIPHY_MIIPHY_REG4C	0x0130	W	0x00000000	mipi phy register 4c
MIIPHY_MIIPHY_REG4D	0x0134	W	0x00000000	mipi phy register 4d
MIIPHY_MIIPHY_REG4E	0x0138	W	0x00000000	mipi phy register 4e
MIIPHY_MIIPHY_REG50	0x0140	W	0x00000000	mipi phy register 50
MIIPHY_MIIPHY_REG51	0x0144	W	0x00000000	mipi phy register 51
MIIPHY_MIIPHY_REG52	0x0148	W	0x00000000	mipi phy register 52
MIIPHY_MIIPHY_REG60	0x0180	W	0x0000000b	mipi phy register 60
MIIPHY_MIIPHY_REG65	0x0194	W	0x00000005	mipi phy register 65
MIIPHY_MIIPHY_REG66	0x0198	W	0x00000000	mipi phy register 66
MIIPHY_MIIPHY_REG67	0x019c	W	0x00000000	mipi phy register 67
MIIPHY_MIIPHY_REG68	0x01a0	W	0x00000000	mipi phy register 68
MIIPHY_MIIPHY_REG69	0x01a4	W	0x00000000	mipi phy register 69
MIIPHY_MIIPHY_REG6A	0x01a8	W	0x00000000	mipi phy register 6a
MIIPHY_MIIPHY_REG6B	0x01ac	W	0x00000000	mipi phy register 6b
MIIPHY_MIIPHY_REG6C	0x01b0	W	0x00000000	mipi phy register 6c
MIIPHY_MIIPHY_REG6D	0x01b4	W	0x00000000	mipi phy register 6d
MIIPHY_MIIPHY_REG6E	0x01b8	W	0x00000000	mipi phy register 6e
MIIPHY_MIIPHY_REG70	0x01c0	W	0x00000000	mipi phy register 70
MIIPHY_MIIPHY_REG71	0x01c4	W	0x00000000	mipi phy register 71
MIIPHY_MIIPHY_REG72	0x01c8	W	0x00000000	mipi phy register 72
MIIPHY_MIIPHY_REG80	0x0200	W	0x0000000b	mipi phy register 80
MIIPHY_MIIPHY_REG85	0x0214	W	0x00000005	mipi phy register 85
MIIPHY_MIIPHY_REG86	0x0218	W	0x00000000	mipi phy register 86
MIIPHY_MIIPHY_REG87	0x021c	W	0x00000000	mipi phy register 87
MIIPHY_MIIPHY_REG88	0x0220	W	0x00000000	mipi phy register 88
MIIPHY_MIIPHY_REG89	0x0224	W	0x00000000	mipi phy register 89

Name	Offset	Size	Reset Value	Description
MIIPHY_MIIPHY_REG8A	0x0228	W	0x00000000	mipi phy register 8a
MIIPHY_MIIPHY_REG8B	0x022c	W	0x00000000	mipi phy register 8b
MIIPHY_MIIPHY_REG8C	0x0230	W	0x00000000	mipi phy register 8c
MIIPHY_MIIPHY_REG8D	0x0234	W	0x00000000	mipi phy register 8d
MIIPHY_MIIPHY_REG8E	0x0238	W	0x00000000	mipi phy register 8e
MIIPHY_MIIPHY_REG90	0x0240	W	0x00000000	mipi phy register 90
MIIPHY_MIIPHY_REG91	0x0244	W	0x00000000	mipi phy register 91
MIIPHY_MIIPHY_REG92	0x0248	W	0x00000000	mipi phy register 92
MIIPHY_MIIPHY_REGA0	0x0280	W	0x0000000b	mipi phy register a0
MIIPHY_MIIPHY_REGA5	0x0294	W	0x00000005	mipi phy register a5
MIIPHY_MIIPHY_REGA6	0x0298	W	0x00000000	mipi phy register a6
MIIPHY_MIIPHY_REGA7	0x029c	W	0x00000000	mipi phy register a7
MIIPHY_MIIPHY_REGA8	0x02a0	W	0x00000000	mipi phy register a8
MIIPHY_MIIPHY_REGA9	0x02a4	W	0x00000000	mipi phy register a9
MIIPHY_MIIPHY_REGAA	0x02a8	W	0x00000000	mipi phy register aa
MIIPHY_MIIPHY_REGAB	0x02ac	W	0x00000000	mipi phy register ab
MIIPHY_MIIPHY_REGAC	0x02b0	W	0x00000000	mipi phy register ac
MIIPHY_MIIPHY_REGAD	0x02b4	W	0x00000000	mipi phy register ad
MIIPHY_MIIPHY_REGAE	0x02b8	W	0x00000000	mipi phy register ae
MIIPHY_MIIPHY_REGB0	0x02c0	W	0x00000000	mipi phy register b0
MIIPHY_MIIPHY_REGB1	0x02c4	W	0x00000000	mipi phy register b1
MIIPHY_MIIPHY_REGB2	0x02c8	W	0x00000000	mipi phy register b2
MIIPHY_MIIPHY_REGC0	0x0300	W	0x0000000b	mipi phy register c0
MIIPHY_MIIPHY_REGC5	0x0314	W	0x00000005	mipi phy register c5
MIIPHY_MIIPHY_REGC6	0x0318	W	0x00000000	mipi phy register c6
MIIPHY_MIIPHY_REGC7	0x031c	W	0x00000000	mipi phy register c7
MIIPHY_MIIPHY_REGC8	0x0320	W	0x00000000	mipi phy register c8
MIIPHY_MIIPHY_REGC9	0x0324	W	0x00000000	mipi phy register c9
MIIPHY_MIIPHY_REGCA	0x0328	W	0x00000000	mipi phy register ca
MIIPHY_MIIPHY_REGCB	0x032c	W	0x00000000	mipi phy register cb
MIIPHY_MIIPHY_REGCC	0x0330	W	0x00000000	mipi phy register cc
MIIPHY_MIIPHY_REGCD	0x0334	W	0x00000000	mipi phy register cd
MIIPHY_MIIPHY_REGCE	0x0338	W	0x00000000	mipi phy register ce
MIIPHY_MIIPHY_REGD0	0x0340	W	0x00000000	mipi phy register d0
MIIPHY_MIIPHY_REGD1	0x0344	W	0x00000000	mipi phy register d1
MIIPHY_MIIPHY_REGD2	0x0348	W	0x00000000	mipi phy register d2

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

8.4.2 Detail Register Description

MIIPHY_MIIPHY_REGO

Address: Operational Base + offset (0x0000)

mipi phy register 0

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	lane_en_ck lane_en_ck 1: enable 0: disable
5	RW	0x0	lane_en_3 lane_en_3 1: enable 0: disable
4	RW	0x0	lane_en_2 lane_en_2 1: enable 0: disable
3	RW	0x0	lane_en_1 lane_en_1 1: enable 0: disable
2	RW	0x0	lane_en_0 lane_en_0 1: enable 0: disable
1	RW	0x0	reserved1 reserved
0	RO	0x1	reserved reserved

MIPIPHY_MIPIPHY_REG1

Address: Operational Base + offset (0x0004)

mipi phy register 1

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	reg_da_syncrst reg_da_syncrst 1: reset 0: normal
1	RW	0x1	reg_da_ldopd reg_da_ldopd 1: power down 0: power on
0	RW	0x1	reg_da_pllpd reg_da_pllpd 1: power down 0: power on

MIPIPHY_MIPIPHY_REG3

Address: Operational Base + offset (0x000c)

mipi phy register 3

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x0	reg_fbdiv reg_fbdiv[8] PLL input reference clock divider
4:0	RW	0x03	reg_prediv reg_prediv[4:0] Integer value programmed into feedback divider

MIPIPHY_MIPIPHY_REG4

Address: Operational Base + offset (0x0010)

mipi phy register 4

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x7d	reg_fbdiv reg_fbdiv[7:0] PLL input reference clock divider

MIIPHY_MIIPHY_REG20

Address: Operational Base + offset (0x0080)

mipi phy register 20

Bit	Attr	Reset Value	Description
31:1	RO	0x0	reserved
0	RW	0x1	reg_dig_rstn reg_dig_rstn 1: normal 0: reset

MIIPHY_MIIPHY_REG40

Address: Operational Base + offset (0x0100)

mipi phy register 40

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0xb	reg_ths_settle Clock Lane Configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. (Can be configured from 4'h0 to 4'hd) 4'b0000 80-110 MHz 4'b0001 110-150 MHz 4'b0010 150-200 MHz 4'b0011 200-250 MHz 4'b0100 250-300 MHz 4'b0101 300-400 MHz 4'b0110 400-500 MHz 4'b0111 500-600 MHz 4'b1000 600-700 MHz 4'b1001 700-800 MHz 4'b1010 800-1000 MHz 4'b1011 additional adjust 4'b1100 additional adjust 4'b1101 additional adjust 4'b1110 additional adjust

MIIPHY_MIIPHY_REG45

Address: Operational Base + offset (0x0114)
mipi phy register 45

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x05	reg_hs_tlp Clock Lane The value of counter for HS Tlp Time ($\geq T_{lp}$) $= T_{pin_txbyteclkhs} * value$

MIPIPHY_MIPIPHY_REG46

Address: Operational Base + offset (0x0118)
mipi phy register 46

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	reg_hs_ths_prepare Clock Lane The value of counter for HS Ths-prepare For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI) $= T_{txddrclkhs} * value$

MIPIPHY_MIPIPHY_REG47

Address: Operational Base + offset (0x011c)
mipi phy register 47

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	reg_hs_the_zero
			Clock Lane
			The value of counter for HS Ths-zero
			For clock lane, Ths-prepare+Ths-zero ($\geq 300\text{ns}$)
			For data lane, Ths-prepare+Ths-zero ($\geq 145\text{ ns} + 10*UI$)
			= Tpin_txbyteclkhs*value
			For clock lane, S_HSTXTHSZERO[5:0] = 6'b100000
			For data lane, S_HSTXTHSZERO[5:0] = 6'b001001
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 3
			110-150 MHz 4
			150-200 MHz 4
			200-250 MHz 5
			250-300 MHz 6
300-400 MHz 7			
400-500 MHz 8			
500-600 MHz 10			
600-700 MHz 11			
700-800 MHz 12			
800-1000 MHz 15			

MIPIPHY_MIPIPHY_REG48

Address: Operational Base + offset (0x0120)

mipi phy register 48

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	reg_hs_ths_trail
			Clock Lane
			The value of counter for HS Ths-trail
			For clock lane, Ths-trail ($\geq 60\text{ns}$)
			For data lane, Ths-trail ($\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$)
			= Tad_txddrclkhs_i* value
			For clock lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			For data lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 12
			110-150 MHz 13
			150-200 MHz 17
			200-250 MHz 20
			250-300 MHz 24
300-400 MHz 29			
400-500 MHz 35			
500-600 MHz 41			
600-700 MHz 49			
700-800 MHz 52			
800-1000 MHz 64			

MIPIPHY_MIPIPHY_REG49

Address: Operational Base + offset (0x0124)

mipi phy register 49

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	reg_hs_ths_exit Clock Lane The value of counter for HS Ths-exit Ths-exit = $T_{\text{pin_txbyteclkhs}} \times \text{value}$

MIPIPHY_MIPIPHY_REG4A

Address: Operational Base + offset (0x0128)

mipi phy register 4a

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	reg_hs_tclk_post Clock Lane The value of counter for HS Tclk-post Tclk-post = Tpin_txbytedkhs*value

MIIPHY_MIIPHY_REG4B

Address: Operational Base + offset (0x012c)

mipi phy register 4b

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reserved Clock Lane reserved

MIIPHY_MIIPHY_REG4C

Address: Operational Base + offset (0x0130)

mipi phy register 4c

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	reg_hs_twakeup Clock Lane The value[9:8] of counter for HS Twakeup also see REG4D

MIIPHY_MIIPHY_REG4D

Address: Operational Base + offset (0x0134)

mipi phy register 4d

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reg_hs_twakeup Clock Lane The value[7:0] of counter for HS Twakeup Twakeup for ulpm, Twakeup = Tpin_sys_clk*value[9:0]

MIIPHY_MIIPHY_REG4E

Address: Operational Base + offset (0x0138)

mipi phy register 4e

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	reg_hs_tclk_pre Clock Lane The value of counter for HS Tclk-pre Tclk-pre for clock lane Tclk-pre = Tpin_txbyteclkhs*value

MIIPHY_MIIPHY_REG50

Address: Operational Base + offset (0x0140)

mipi phy register 50

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_go Clock Lane The value of counter for HS Tta-go Tta-go for turnaround Tta-go = Ttxclkesc*value

MIIPHY_MIIPHY_REG51

Address: Operational Base + offset (0x0144)

mipi phy register 51

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_sure Clock Lane The value of counter for HS Tta-sure Tta-sure for turnaround Tta-sure = Ttxclkesc*value

MIIPHY_MIIPHY_REG52

Address: Operational Base + offset (0x0148)

mipi phy register 52

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_wait Clock Lane The value of counter for HS Tta-wait Tta-wait for turnaround Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value

MIPIPHY_MIPIPHY_REG60

Address: Operational Base + offset (0x0180)

mipi phy register 60

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0xb	reg_ths_settle Data0 Lane Configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. (Can be configured from 4'h0 to 4'hd) 4'b0000 80-110 MHz 4'b0001 110-150 MHz 4'b0010 150-200 MHz 4'b0011 200-250 MHz 4'b0100 250-300 MHz 4'b0101 300-400 MHz 4'b0110 400-500 MHz 4'b0111 500-600 MHz 4'b1000 600-700 MHz 4'b1001 700-800 MHz 4'b1010 800-1000 MHz 4'b1011 additional adjust 4'b1100 additional adjust 4'b1101 additional adjust 4'b1110 additional adjust

MIPIPHY_MIPIPHY_REG65

Address: Operational Base + offset (0x0194)

mipi phy register 65

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x05	reg_hs_tlp Data0 Lane The value of counter for HS Tlp Time ($\geq T_{lp}$) $= T_{pin_txbyteclkhs} * value$

MIPIPHY_MIPIPHY_REG66

Address: Operational Base + offset (0x0198)

mipi phy register 66

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	reg_hs_ths_prepare Data0 Lane The value of counter for HS Ths-prepare For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI) $= T_{txddrclkhs} * value$

MIPIPHY_MIPIPHY_REG67

Address: Operational Base + offset (0x019c)

mipi phy register 67

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	reg_hs_the_zero
			Data0 Lane
			The value of counter for HS Ths-zero
			For clock lane, Ths-prepare+Ths-zero ($\geq 300\text{ns}$)
			For data lane, Ths-prepare+Ths-zero ($\geq 145\text{ ns} + 10*UI$)
			= $T_{pin_txbyteclkhs}*\text{value}$
			For clock lane, S_HSTXTHSZERO[5:0] = 6'b100000
			For data lane, S_HSTXTHSZERO[5:0] = 6'b001001
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 3
			110-150 MHz 4
			150-200 MHz 4
			200-250 MHz 5
			250-300 MHz 6
300-400 MHz 7			
400-500 MHz 8			
500-600 MHz 10			
600-700 MHz 11			
700-800 MHz 12			
800-1000 MHz 15			

MIPIPHY_MIPIPHY_REG68

Address: Operational Base + offset (0x01a0)

mipi phy register 68

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	reg_hs_ths_trail
			Data0 Lane
			The value of counter for HS Ths-trail
			For clock lane, Ths-trail ($\geq 60\text{ns}$)
			For data lane, Ths-trail ($\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$)
			= Tad_txddrclkhs_i* value
			For clock lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			For data lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 12
			110-150 MHz 13
			150-200 MHz 17
			200-250 MHz 20
			250-300 MHz 24
300-400 MHz 29			
400-500 MHz 35			
500-600 MHz 41			
600-700 MHz 49			
700-800 MHz 52			
800-1000 MHz 64			

MIPIPHY_MIPIPHY_REG69

Address: Operational Base + offset (0x01a4)

mipi phy register 69

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	reg_hs_ths_exit Data0 Lane The value of counter for HS Ths-exit Ths-exit = $T_{\text{pin_txbyteclkhs}} \times \text{value}$

MIPIPHY_MIPIPHY_REG6A

Address: Operational Base + offset (0x01a8)

mipi phy register 6a

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	reg_hs_tclk_post Data0 Lane The value of counter for HS Tclk-post Tclk-post = Tpin_txbytedkhs*value

MIIPHY_MIIPHY_REG6B

Address: Operational Base + offset (0x01ac)

mipi phy register 6b

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reserved Data0 Lane reserved

MIIPHY_MIIPHY_REG6C

Address: Operational Base + offset (0x01b0)

mipi phy register 6c

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	reg_hs_twakeup Data0 Lane The value[9:8] of counter for HS Twakeup also see REG6D

MIIPHY_MIIPHY_REG6D

Address: Operational Base + offset (0x01b4)

mipi phy register 6d

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reg_hs_twakeup Data0 Lane The value[7:0] of counter for HS Twakeup Twakeup for ulpm, Twakeup = Tpin_sys_clk*value[9:0]

MIIPHY_MIIPHY_REG6E

Address: Operational Base + offset (0x01b8)

mipi phy register 6e

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	reg_hs_tclk_pre Data0 Lane The value of counter for HS Tclk-pre Tclk-pre for clock lane Tclk-pre = Tpin_txbyteclkhs*value

MIIPHY_MIIPHY_REG70

Address: Operational Base + offset (0x01c0)

mipi phy register 70

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_go Data0 Lane The value of counter for HS Tta-go Tta-go for turnaround Tta-go = Ttxclkesc*value

MIIPHY_MIIPHY_REG71

Address: Operational Base + offset (0x01c4)

mipi phy register 71

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_sure Data0 Lane The value of counter for HS Tta-sure Tta-sure for turnaround Tta-sure = Ttxclkesc*value

MIIPHY_MIIPHY_REG72

Address: Operational Base + offset (0x01c8)

mipi phy register 72

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_wait Data0 Lane The value of counter for HS Tta-wait Tta-wait for turnaround Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value

MIPIPHY_MIPIPHY_REG80

Address: Operational Base + offset (0x0200)

mipi phy register 80

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0xb	reg_ths_settle Data1 Lane Configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. (Can be configured from 4'h0 to 4'hd) 4'b0000 80-110 MHz 4'b0001 110-150 MHz 4'b0010 150-200 MHz 4'b0011 200-250 MHz 4'b0100 250-300 MHz 4'b0101 300-400 MHz 4'b0110 400-500 MHz 4'b0111 500-600 MHz 4'b1000 600-700 MHz 4'b1001 700-800 MHz 4'b1010 800-1000 MHz 4'b1011 additional adjust 4'b1100 additional adjust 4'b1101 additional adjust 4'b1110 additional adjust

MIPIPHY_MIPIPHY_REG85

Address: Operational Base + offset (0x0214)

mipi phy register 85

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x05	reg_hs_tlp Data1 Lane The value of counter for HS Tlp Time ($\geq T_{lp}$) $= T_{pin_txbyteclkhs} * value$

MIPIPHY_MIPIPHY_REG86

Address: Operational Base + offset (0x0218)

mipi phy register 86

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	reg_hs_ths_prepare Data1 Lane The value of counter for HS Ths-prepare For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI) $= T_{txddrclkhs} * value$

MIPIPHY_MIPIPHY_REG87

Address: Operational Base + offset (0x021c)

mipi phy register 87

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	reg_hs_the_zero
			Data1 Lane
			The value of counter for HS Ths-zero
			For clock lane, Ths-prepare+Ths-zero ($\geq 300\text{ns}$)
			For data lane, Ths-prepare+Ths-zero ($\geq 145\text{ ns} + 10*UI$)
			= Tpin_txbyteclkhs*value
			For clock lane, S_HSTXTHSZERO[5:0] = 6'b100000
			For data lane, S_HSTXTHSZERO[5:0] = 6'b001001
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 3
			110-150 MHz 4
			150-200 MHz 4
			200-250 MHz 5
			250-300 MHz 6
300-400 MHz 7			
400-500 MHz 8			
500-600 MHz 10			
600-700 MHz 11			
700-800 MHz 12			
800-1000 MHz 15			

MIPIPHY_MIPIPHY_REG88

Address: Operational Base + offset (0x0220)

mipi phy register 88

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	reg_hs_ths_trail
			Data1 Lane
			The value of counter for HS Ths-trail
			For clock lane, Ths-trail ($\geq 60\text{ns}$)
			For data lane, Ths-trail ($\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$)
			= Tad_txddrclkhs_i* value
			For clock lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			For data lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 12
			110-150 MHz 13
			150-200 MHz 17
			200-250 MHz 20
			250-300 MHz 24
300-400 MHz 29			
400-500 MHz 35			
500-600 MHz 41			
600-700 MHz 49			
700-800 MHz 52			
800-1000 MHz 64			

MIPIPHY_MIPIPHY_REG89

Address: Operational Base + offset (0x0224)

mipi phy register 89

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	reg_hs_ths_exit Data1 Lane The value of counter for HS Ths-exit Ths-exit = $T_{\text{pin_txbyteclkhs}} \times \text{value}$

MIPIPHY_MIPIPHY_REG8A

Address: Operational Base + offset (0x0228)

mipi phy register 8a

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	reg_hs_tclk_post Data1 Lane The value of counter for HS Tclk-post Tclk-post = Tpin_txbytedkhs*value

MIIPHY_MIIPHY_REG8B

Address: Operational Base + offset (0x022c)

mipi phy register 8b

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reserved Data1 Lane reserved

MIIPHY_MIIPHY_REG8C

Address: Operational Base + offset (0x0230)

mipi phy register 8c

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	reg_hs_twakeup Data1 Lane The value[9:8] of counter for HS Twakeup also see REG8D

MIIPHY_MIIPHY_REG8D

Address: Operational Base + offset (0x0234)

mipi phy register 8d

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reg_hs_twakeup Data1 Lane The value[7:0] of counter for HS Twakeup Twakeup for ulpm, Twakeup = Tpin_sys_clk*value[9:0]

MIIPHY_MIIPHY_REG8E

Address: Operational Base + offset (0x0238)

mipi phy register 8e

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	reg_hs_tclk_pre Data1 Lane The value of counter for HS Tclk-pre Tclk-pre for clock lane Tclk-pre = Tpin_txbyteclkhs*value

MIIPHY_MIIPHY_REG90

Address: Operational Base + offset (0x0240)

mipi phy register 90

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_go Data1 Lane The value of counter for HS Tta-go Tta-go for turnaround Tta-go = Ttxclkesc*value

MIIPHY_MIIPHY_REG91

Address: Operational Base + offset (0x0244)

mipi phy register 91

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_sure Data1 Lane The value of counter for HS Tta-sure Tta-sure for turnaround Tta-sure = Ttxclkesc*value

MIIPHY_MIIPHY_REG92

Address: Operational Base + offset (0x0248)

mipi phy register 92

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_wait Data1 Lane The value of counter for HS Tta-wait Tta-wait for turnaround Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value

MIPIPHY_MIPIPHY_REGA0

Address: Operational Base + offset (0x0280)

mipi phy register a0

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0xb	reg_ths_settle Data2 Lane Configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. (Can be configured from 4'h0 to 4'hd) 4'b0000 80-110 MHz 4'b0001 110-150 MHz 4'b0010 150-200 MHz 4'b0011 200-250 MHz 4'b0100 250-300 MHz 4'b0101 300-400 MHz 4'b0110 400-500 MHz 4'b0111 500-600 MHz 4'b1000 600-700 MHz 4'b1001 700-800 MHz 4'b1010 800-1000 MHz 4'b1011 additional adjust 4'b1100 additional adjust 4'b1101 additional adjust 4'b1110 additional adjust

MIIPHY_MIIPHY_REGA5

Address: Operational Base + offset (0x0294)

mipi phy register a5

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x05	reg_hs_tlp Data2 Lane The value of counter for HS Tlp Time ($\geq T_{lp}$) $= T_{pin_txbyteclkhs} * value$

MIIPHY_MIIPHY_REGA6

Address: Operational Base + offset (0x0298)

mipi phy register a6

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	reg_hs_ths_prepare Data2 Lane The value of counter for HS Ths-prepare For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI) $= T_{txddrclkhs} * value$

MIIPHY_MIIPHY_REGA7

Address: Operational Base + offset (0x029c)

mipi phy register a7

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	reg_hs_the_zero
			Data2 Lane
			The value of counter for HS Ths-zero
			For clock lane, Ths-prepare+Ths-zero ($\geq 300\text{ns}$)
			For data lane, Ths-prepare+Ths-zero ($\geq 145\text{ ns} + 10*UI$)
			= Tpin_txbyteclkhs*value
			For clock lane, S_HSTXTHSZERO[5:0] = 6'b100000
			For data lane, S_HSTXTHSZERO[5:0] = 6'b001001
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 3
			110-150 MHz 4
			150-200 MHz 4
			200-250 MHz 5
			250-300 MHz 6
300-400 MHz 7			
400-500 MHz 8			
500-600 MHz 10			
600-700 MHz 11			
700-800 MHz 12			
800-1000 MHz 15			

MIPIPHY_MIPIPHY_REGA8

Address: Operational Base + offset (0x02a0)

mipi phy register a8

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	reg_hs_ths_trail
			Data2 Lane
			The value of counter for HS Ths-trail
			For clock lane, Ths-trail ($\geq 60\text{ns}$)
			For data lane, Ths-trail ($\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$)
			= Tad_txddrclkhs_i* value
			For clock lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			For data lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 12
			110-150 MHz 13
			150-200 MHz 17
			200-250 MHz 20
			250-300 MHz 24
300-400 MHz 29			
400-500 MHz 35			
500-600 MHz 41			
600-700 MHz 49			
700-800 MHz 52			
800-1000 MHz 64			

MIPIPHY_MIPIPHY_REGA9

Address: Operational Base + offset (0x02a4)

mipi phy register a9

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	reg_hs_ths_exit Data2 Lane The value of counter for HS Ths-exit Ths-exit = $T_{\text{pin_txbyteclkhs}} \times \text{value}$

MIPIPHY_MIPIPHY_REGAA

Address: Operational Base + offset (0x02a8)

mipi phy register aa

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	reg_hs_tclk_post Data2 Lane The value of counter for HS Tclk-post Tclk-post = Tpin_txbytedkhs*value

MIIPHY_MIIPHY_REGAB

Address: Operational Base + offset (0x02ac)

mipi phy register ab

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reserved Data2 Lane reserved

MIIPHY_MIIPHY_REGAC

Address: Operational Base + offset (0x02b0)

mipi phy register ac

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	reg_hs_twakeup Data2 Lane The value[9:8] of counter for HS Twakeup also see REGAD

MIIPHY_MIIPHY_REGAD

Address: Operational Base + offset (0x02b4)

mipi phy register ad

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reg_hs_twakeup Data2 Lane The value[7:0] of counter for HS Twakeup Twakeup for ulpm, Twakeup = Tpin_sys_clk*value[9:0]

MIIPHY_MIIPHY_REGAE

Address: Operational Base + offset (0x02b8)

mipi phy register ae

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	reg_hs_tclk_pre Data2 Lane The value of counter for HS Tclk-pre Tclk-pre for clock lane Tclk-pre = Tpin_txbyteclkhs*value

MIIPHY_MIIPHY_REGB0

Address: Operational Base + offset (0x02c0)

mipi phy register b0

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_go Data2 Lane The value of counter for HS Tta-go Tta-go for turnaround Tta-go = Ttxclkesc*value

MIIPHY_MIIPHY_REGB1

Address: Operational Base + offset (0x02c4)

mipi phy register b1

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_sure Data2 Lane The value of counter for HS Tta-sure Tta-sure for turnaround Tta-sure = Ttxclkesc*value

MIIPHY_MIIPHY_REGB2

Address: Operational Base + offset (0x02c8)

mipi phy register b2

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_wait Data2 Lane The value of counter for HS Tta-wait Tta-wait for turnaround Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value

MIPIPHY_MIPIPHY_REGC0

Address: Operational Base + offset (0x0300)

mipi phy register c0

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0xb	reg_ths_settle Data3 Lane Configure the count time of the THS-SETTLE by protocol. After the count done, D-PHY will begin to receive the high speed data. (Can be configured from 4'h0 to 4'hd) 4'b0000 80-110 MHz 4'b0001 110-150 MHz 4'b0010 150-200 MHz 4'b0011 200-250 MHz 4'b0100 250-300 MHz 4'b0101 300-400 MHz 4'b0110 400-500 MHz 4'b0111 500-600 MHz 4'b1000 600-700 MHz 4'b1001 700-800 MHz 4'b1010 800-1000 MHz 4'b1011 additional adjust 4'b1100 additional adjust 4'b1101 additional adjust 4'b1110 additional adjust

MIPIPHY_MIPIPHY_REGC5

Address: Operational Base + offset (0x0314)

mipi phy register c5

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x05	reg_hs_tlp Data3 Lane The value of counter for HS Tlp Time ($\geq T_{lp}$) $= T_{pin_txbyteclkhs} * value$

MIPIPHY_MIPIPHY_REGC6

Address: Operational Base + offset (0x0318)

mipi phy register c6

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6:0	RW	0x00	reg_hs_ths_prepare Data3 Lane The value of counter for HS Ths-prepare For clock lane, Ths-prepare(38ns~95ns) For data lane, Ths-prepare(40ns+4UI~85ns+6UI) $= T_{txddrclkhs} * value$

MIPIPHY_MIPIPHY_REGC7

Address: Operational Base + offset (0x031c)

mipi phy register c7

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	reg_hs_the_zero
			Data3 Lane
			The value of counter for HS Ths-zero
			For clock lane, Ths-prepare+Ths-zero ($\geq 300\text{ns}$)
			For data lane, Ths-prepare+Ths-zero ($\geq 145\text{ ns} + 10*UI$)
			= Tpin_txbyteclkhs*value
			For clock lane, S_HSTXTHSZERO[5:0] = 6'b100000
			For data lane, S_HSTXTHSZERO[5:0] = 6'b001001
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 3
			110-150 MHz 4
			150-200 MHz 4
			200-250 MHz 5
			250-300 MHz 6
300-400 MHz 7			
400-500 MHz 8			
500-600 MHz 10			
600-700 MHz 11			
700-800 MHz 12			
800-1000 MHz 15			

MIPIPHY_MIPIPHY_REGC8

Address: Operational Base + offset (0x0320)

mipi phy register c8

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6:0	RW	0x00	reg_hs_ths_trail
			Data3 Lane
			The value of counter for HS Ths-trail
			For clock lane, Ths-trail ($\geq 60\text{ns}$)
			For data lane, Ths-trail ($\geq \max(8\text{UI}, 60\text{ns}+4\text{UI})$)
			= Tad_txddrclkhs_i* value
			For clock lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			For data lane, S_HXTXTHSTRAIL[6:0] = 7'b0100111
			Frequency(1/UI) Value(Decimal)
			80 -110 MHz 12
			110-150 MHz 13
			150-200 MHz 17
			200-250 MHz 20
			250-300 MHz 24
300-400 MHz 29			
400-500 MHz 35			
500-600 MHz 41			
600-700 MHz 49			
700-800 MHz 52			
800-1000 MHz 64			

MIPIPHY_MIPIPHY_REGC9

Address: Operational Base + offset (0x0324)

mipi phy register c9

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4:0	RW	0x00	reg_hs_ths_exit Data3 Lane The value of counter for HS Ths-exit Ths-exit = $T_{\text{pin_txbyteclkhs}} \times \text{value}$

MIPIPHY_MIPIPHY_REGCA

Address: Operational Base + offset (0x0328)

mipi phy register ca

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3:0	RW	0x0	reg_hs_tclk_post Data3 Lane The value of counter for HS Tclk-post Tclk-post = Tpin_txbytedkhs*value

MIIPHY_MIIPHY_REGCB

Address: Operational Base + offset (0x032c)

mipi phy register cb

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reserved Data3 Lane reserved

MIIPHY_MIIPHY_REGCC

Address: Operational Base + offset (0x0330)

mipi phy register cc

Bit	Attr	Reset Value	Description
31:2	RO	0x0	reserved
1:0	RW	0x0	reg_hs_twakeup Data3 Lane The value[9:8] of counter for HS Twakeup also see REGCD

MIIPHY_MIIPHY_REGCD

Address: Operational Base + offset (0x0334)

mipi phy register cd

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x00	reg_hs_twakeup Data3 Lane The value[7:0] of counter for HS Twakeup Twakeup for ulpm, Twakeup = Tpin_sys_clk*value[9:0]

MIIPHY_MIIPHY_REGCE

Address: Operational Base + offset (0x0338)

mipi phy register ce

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:0	RW	0x0	reg_hs_tclk_pre Data3 Lane The value of counter for HS Tclk-pre Tclk-pre for clock lane Tclk-pre = Tpin_txbyteclkhs*value

MIIPHY_MIIPHY_REGD0

Address: Operational Base + offset (0x0340)

mipi phy register d0

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_go Data3 Lane The value of counter for HS Tta-go Tta-go for turnaround Tta-go = Ttxclkesc*value

MIIPHY_MIIPHY_REGD1

Address: Operational Base + offset (0x0344)

mipi phy register d1

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_sure Data3 Lane The value of counter for HS Tta-sure Tta-sure for turnaround Tta-sure = Ttxclkesc*value

MIIPHY_MIIPHY_REGD2

Address: Operational Base + offset (0x0348)

mipi phy register d2

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:0	RW	0x00	reg_hs_tta_wait Data3 Lane The value of counter for HS Tta-wait Tta-wait for turnaround Interval from receiving ppi turnaround request to sending esc request. Tta-wait = Ttxclkesc*value

8.5 Interface Timing

This section shows a PPI timing relationship at high-speed transmission. While pin_txrequesths is low, the Lane Module ignores the value of pin_txdatahs. To begin the transmission, the protocol drives pin_txdatahs with the first byte of data and asserts pin_txrequesths. This data byte is accepted by the PHY on the first rising edge of pin_txbyteclkhs with pin_txreadyhs also asserted. At this point, the protocol logic drives the next data byte onto pin_txdatahs. After every rising clock cycle with pin_txreadyhs active, the protocol supplies a new valid data byte or ends the transmission. After the last data byte has been transferred to the Lane Module, pin_txrequesths is driven low to cause the Lane Module to stop the transmission and enter Stop state. The minimum number of bytes transmitted could be as small as one.

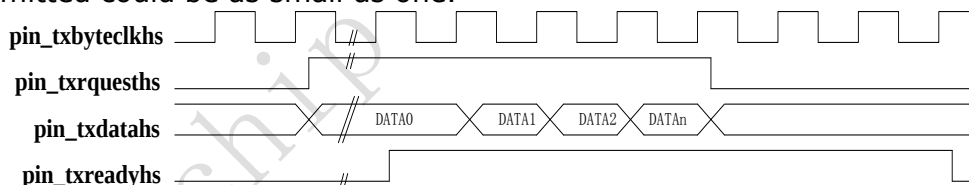


Fig. 8-3HS-TX PPI Timing

This section shows a PPI timing relationship at low-power data transmission operation. The Protocol directs the Data Lane to enter Low-Power data transmission Escape mode by asserting pin_txrequestesc with pin_txlpdtesc high. The Low-Power transmit data is transferred on the pin_txdataesc lines when pin_txvalidesc and pin_txreadyesc are both active at a rising edge of pin_txclkesc.

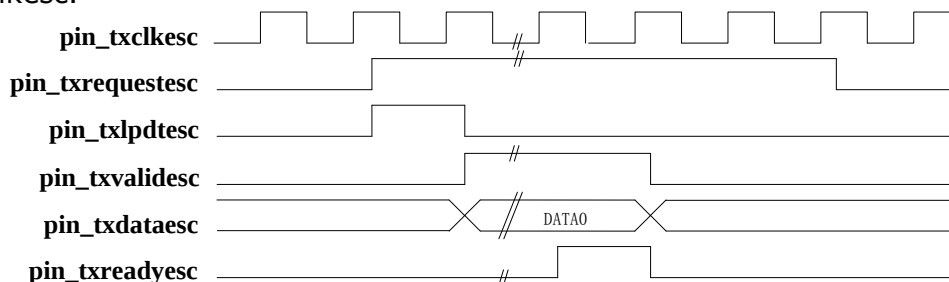


Fig. 8-4LPDT TX PPI Timing

This section shows a PPI timing relationship at low-power data reception. The signal pin_rxlpdtesc is asserted when the escape entry command is detected and stays high until the Lane returns to stop state, indicating that the transmission has finished.

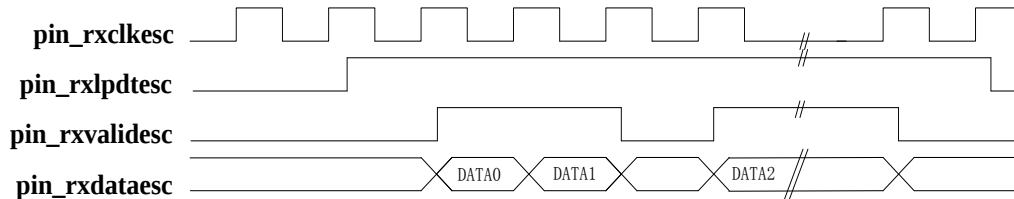


Fig. 8-5LPDT RX PPI Timing

8.6 Application Notes

8.6.1 Low power mode

Low Power Mode is a special feature for D-PHY. You can control this function by using proper registers from the Innosilicon D-PHY with few operations. The following is a step by step instruction for low power mode in and out.

Low Power in Steps:

- Step1: Send 0x01 to register 0x00. Disable all lanes on analog part.
- Step2: Send 0xe3 to register 0x01. Disable PLL and LDO.
- Step3: Wait a period before reference clock have been disabled.
- Step4: Disable reference clock.

Low Power out Steps:

- Step1: Enable reference clock.
- Step2: Wait a period after reference clock have been enabled.
- Step3: Send 0xe4 to register 0x01. Enable PLL and LDO.
- Step4: Send 0x7d to register 0x00. Enable all lanes on analog part.
- Step5: Send 0xe0 to register 0x01. Reset analog.
- Step6: Wait a period after analog has been reset.
- Step7: Send 0x1e to register 0x20. Reset digital.
- Step8: Send 0x1f to register 0x20. Reset digital.
- Step9: Wait a period before normal transmission.

8.6.2 Programmable PLL IN DSI TX

Frequency Calculating Formula

The PLL output frequency can be calculated using a simple formula:

$$\text{PLL_Output_Frequency} = \text{FREF} / \text{PREDIV} * \text{FBDIV}$$

PLL_Output_Frequency: It is equal to DDR- Clock-Frequency * 2

FREF : PLL input reference frequency which equals to the frequency of the pin_clkhtref

PREDIV : PLL input reference clock divider which can be configured by the register of reg_prediv

FBDIV : Integer value programmed into feedback divider which can be configured by the register of reg_fbdiv

For example,

FREF =20MHz, PLL output frequency = 800Hz, so set PREDIV=1, FBDIV=40

Additional Programming Considerations

1. The divided reference frequency (FREF/PREDIV) should be less than 40MHz.
2. The all possible settings of feedback divider are 12,13,14,16~511.

8.7 ELECTRICAL SPECIFICATIONS

8.7.1 DC SPECIFICATIONS

Table 8-1 HS Transmitter DC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V _{CMTX}	HS TX static Common-mode voltage	150	200	250	mV	1
$\Delta V_{CMTX(1,0)}$	V _{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	2
V _{OD}	HS transmit differential voltage	140	200	270	mV	1
ΔV_{OD}	V _{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2
V _{OHHS}	HS output high voltage			360	mV	1
Z _{os}	Single ended output impedance	40	50	62.5	ohm	
ΔZ_{os}	Single ended output impedance mismatch			10	%	

1. Value when driving into load impedance anywhere in the ZID range.
2. It is recommended the implementer minimize ΔV_{OD} and $\Delta V_{CMTX(1,0)}$ in order to minimize radiation and optimize signal integrity.

Table 8-2 HS Transmitter DC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V _{IH}	Logic 1 input voltage	880			mV	
V _{IL}	Logic 0 input voltage, not in ULP State			550	mV	
V _{IL-ULPS}	Logic 0 input voltage, ULP State			300	mV	
V _{HYST}	Input hysteresis	25			mV	

Table 8-3 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Unit	Note
V _{OH}	The venin output high level	1.1	1.2	1.3	V	
V _{OL}	The venin output low level	-50		50	mV	
Z _{OLP}	Output impedance of LP transmitter	110			Ω	1

1. Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the TRLP/TFLP specification is met.

8.7.2 AC specifications

Table 8-4 HS receiver AC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
ΔV _{CMRX} (HF)	Common-mode interference beyond 450 MHz			100	mV	2
ΔV _{CMRX} (LF)	Common-mode interference 50MHz – 450MHz	-50		50	mV	1,4
C _{CM}	Common-mode termination			60	pF	3

1. Excluding 'static' ground shift of 50mV
2. ΔV_{CMRX}(HF) is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.
4. Voltage difference compared to the DC average common-mode potential.

Table 8-5 LP receiver AC specifications

Parameter	Description	Min	Nom	Max	Unit	Note
e _{SPIKE}	Input pulse rejection			300	V.ps	1, 2,3
T _{MIN-RX}	Minimum pulse width response	20			ns	4
V _{INT}	Peak interference amplitude			200	mV	
f _{INT}	Interference frequency	450			MHz	

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Table 8-6 LP Transmitter AC specifications

Paramete	Description	Min	No	Ma	Unit	Note
----------	-------------	-----	----	----	------	------

r			m	x		
T _{RLP} /T _{FLP}	15%-85% rise time and fall time			25	ns	1
T _{REOT}	30%-85% rise time and fall time			35	ns	1,5,6
T _{LTP-PULSE-TX}	Pulse width of exclusive-OR clock the LP	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40		ns	4
		All other pulses	20			4
T _{LTP-PER-TX}	Period of the LP exclusive-OR clock		90		ns	
δV/δt _{SR}	Slew rate @ C _{LOAD} = 0pF			500	mV/ns	1,3,7,8
	Slew rate @ C _{LOAD} = 5pF			300	mV/ns	1,3,7,8
	Slew rate @ C _{LOAD} = 20pF			250	mV/ns	1,3,7,8
	Slew rate @ C _{LOAD} = 70pF			150	mV/ns	1,3,7,8
	Slew rate @ C _{LOAD} = 0 to 70pF(Falling Edge Only)		30		mV/ns	1,2,3
	Slew rate @ C _{LOAD} = 0 to 70pF(Rising Edge Only)		30		mV/ns	1,3,9
	Slew rate @ C _{LOAD} = 0 to 70pF(Rising Edge Only)		30-0.075 * (V _{O,INST} - 700)		mV/ns	1,10,11
C _{LOAD}	Load capacitance		0	70	pF	1

1. C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.
2. When the output voltage is between 400 mV and 930 mV.
3. Measured as average across any 50 mV segment of the output signal transition.
4. This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in section 8.2.2.
5. The rise-time of TREOT starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.
6. With an additional load capacitance CCM between 0 and 60pF on the termination center tap at RX side of the Lane
7. This value represents a corner point in a piecewise linear curve.

8. When the output voltage is in the range specified by VPIN(absmax).
9. When the output voltage is between 400 mV and 700 mV.
10. Where VO,INST is the instantaneous output voltage, VDP or VDN, in millivolts.
11. When the output voltage is between 700 mV and 930 mV.

Rockchip Confidential

Chapter 9 LVDS

9.1 Overview

LVDS transmitter converts a CMOS signal into a low-voltage differential signal. Using a differential signal reduces the system's susceptibility to noise and EMI emissions. In addition, using a differential signal can deliver high speeds. This results in a very cost-effective solution to some of the greatest bandwidth bottlenecks in many transmission applications.

LVDS offers designers flexibility around their power supply solution, working equally well at 3.3V and lower. As a result, designers can reuse their LVDS solution even as systems move to lower voltages.

The LVDS transmitter in jettaplus supports both single channel and dual channel.

9.1.1 Features

- 150MHz clock support
- Support single pixel and dual pixel interface
- 28:4 data sub_channel compression at data rate up to 1050Mbps per channel
- Support VGA, SVGA, XGA, SXGA and SXGA+
- PLL requires no external components
- LVTTTL Combo I/O, support LVDS/TTL data output
- LVDS mode supply voltage: 1.2V/2.5V; LVTTTL mode supply voltage: 1.2V/3.3V
- Comply with the Standard TIA/EIA-644-A LVDS standard

9.2 Block Diagram

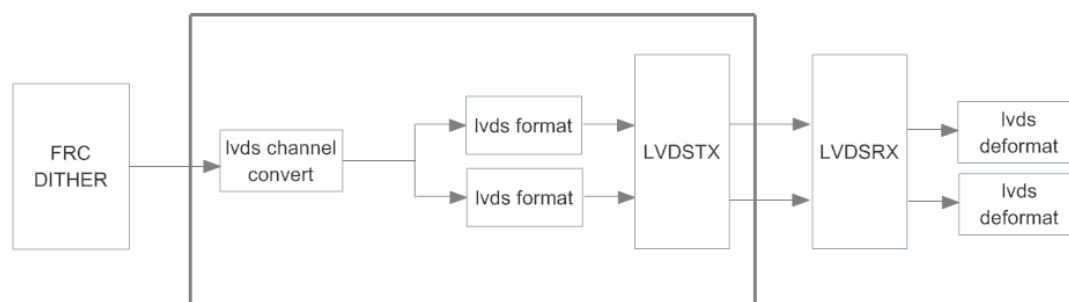


Fig. 9-1 LVDS Block Diagram

9.3 Function description

9.3.1 lvds channel convert

lvds_channel_convert converts 24-bit RGB signal to two group 24-bit RGB

signals.

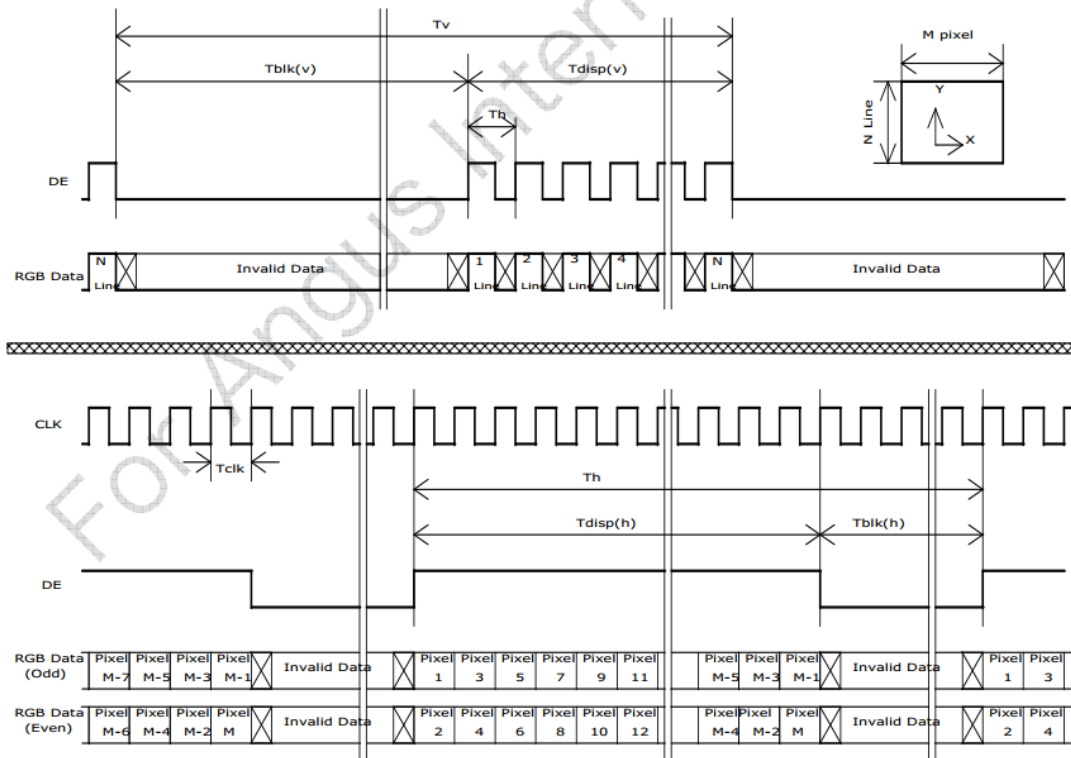


Fig. 9-2lvds_channel_convertTiming

9.3.2 Truth table of LVDS Transmitter

Table9-1Truth Table of LVDS Transmitter

MODE	INPUT								OUTPUT	
	PDN_CBG	PD_PLL	PDN_1	OEN_1	PDN_2	OEN_2	Dn_m	Tq (1-20)	PADP/N_n &CLKP/N1 (n=1-4)	PADP/N_n &CLKP/N2 (n=5-8)
Dual LVDS Output	1	0	1	0	1	0	X	X	Refer to Figure 2	Refer to Figure 2
Single LVDS Output (CH1)	1	0	1	0	0	0	X	X	Refer to Figure 2	Z
LVTTL Output (CH1&2)	0	1	0	1	0	1	X	X	Tq (q=1~10)	Tq (q=11~20)
LVTTL Output (CH1)	0	1	0	1	0	0	X	X	Tq (q=1~10)	Z
Output Disable	x	0	0	0	0	0	X	X	Z	Z
Power Down	0	1	0	0	0	0	X	X	Z	Z

In default or after reset, LVDS Transmitter is in Power Down.

9.3.3 DC and AC Specification

This section provides DC and AC information of LVDS Transmitter. It includes the absolute maximum rating conditions for 2.5V(LVDS output mode) I/O application in Table22-2 and 3.3V(LVTTL output mode) I/O application in Table22-3 ,absolute maximum rating condition can either caused device reliability problem or damage the device sufficiently to cause immediate failure. Transmitter DC electrical specifications are showed in Table22-4. AC specifications are characterized in three operating condition. Those are worst-case, typical-case and best-case conditions and the detail of each condition are listed in the Table22-5 and Table22-6 and AC electrical specifications of transmitter are showed in Table22-7.

Please be kindly reminded that the LVDS output mode could only work under 2.5V I/O application, and LVTTL output mode works under 3.3V I/O application.

Table9-2Absolute Maximum Rating for 2.5V LVDS Output Application

Symbol	Parameter	Conditions	Minimum	Normal	Maximum
VDDDLVD	LVDS post-driver analog power		2.25V	2.5V	2.75V
VDDPLVD	LVDS level shifter power		2.25V	2.5V	2.75V
VDDPLL	PLL power		2.25V	2.5V	2.75V
VDD	LVDS & Serializer pre-driver power	±10%	1.08V	1.2V	1.32V
V _O	Pad output voltage (PADP_n, PADN_n)		0V	VDDDLVD	2.75V
V _{IC}	Core input voltage (Dn_m, OEN_n, PDN_n)		0V	VDD	1.32V
T _{OPT}	Operating temperature		0°C	25°C	125°C

Table9-3Absolute Maximum Rating for 3.3V LVTTL Output Application

Symbol	Parameter	Conditions	Minimum	Normal	Maximum
VDDDLVD	LVDS post-driver analog power		2.97V	3.3V	3.63V
VDDPLVD	LVDS level shifter power		2.97V	3.3V	3.63V
VDDPLL	PLL power		2.97V	3.3V	3.63V
VDD	LVDS & Serializer pre-driver power	±10%	1.08V	1.2V	1.32V
V _O	Pad output voltage (PADP_n, PADN_n)		0V	VDDDLVD	3.63V
V _{IC}	Core input voltage (Dn_m, OEN_n, PDN_n)		0V	VDD	1.32V
T _{OPT}	Operating temperature		0°C	25°C	125°C

Table9-4LVDS Transmitter DC Electrical Specifications

Symbol	Parameter	Conditions	Minimum	Maximum
V_{oh}	Output voltage high, V_{oa} or V_{ob}	$R_{load} = 100\Omega \pm 1\%$		1475mV
V_{ol}	Output voltage low, V_{oa} or V_{ob}	$R_{load} = 100\Omega \pm 1\%$	925mV	
$ V_{od} $	Output differential voltage	$R_{load} = 100\Omega \pm 1\%$	250mV	450mV
V_{os}	Output offset voltage	$R_{load} = 100\Omega \pm 1\%$	1125mV	1375mV
$ \Delta V_{od} $	Change in $ V_{od} $ between '0' and '1'	$R_{load} = 100\Omega \pm 1\%$		50mV/150mV#
ΔV_{os}	Change in V_{os} between '0' and '1'	$R_{load} = 100\Omega \pm 1\%$		50mV
I_{sa}, I_{sb}	Output current	Transmitter shorted to ground		24mA
I_{sab}	Output current	Transmitter shorted to ground		12mA

Table9-5LVDS Transmitter AC Characterization Condition for 2.5V I/O Application

Type	Condition
Typical case	VDDDLVD=2.5V, VDDPLVD=2.5V, VDDPLL=2.5V, VDD=1.2V, temperature=25℃ Process = Typical-Typical
Best case	VDDDLVD=2.75V, VDDPLVD=2.75V, VDDPLL=2.75V, VDD=1.32V temperature=0℃ Process = Fast-Fast
Best case (High temperature)	VDDDLVD=2.75V, VDDPLVD=2.75V, VDDPLL=2.75V, VDD=1.32V temperature=125℃ Process = Fast-Fast
Best case (Low temperature)	VDDDLVD=2.75V, VDDPLVD=2.75V, VDDPLL=2.75V, VDD=1.32V temperature=-40℃ Process = Fast-Fast
Worst case (High temperature)	VDDDLVD=2.25V, VDDPLVD=2.25V, VDDPLL=2.25V, VDD=1.08V temperature=125℃ Process =Slow-Slow
Worst Case (Low temperature)	VDDDLVD=2.25V, VDDPLVD=2.25V, VDDPLL=2.25V, VDD=1.08V temperature=-40℃ Process =Slow-Slow

Table9-6LVDS Transmitter AC Characterization Condition for 3.3V I/O Application

Type	Condition
Typical case	VDDDLVD=3.3V, VDDPLVD=3.3V, VDDPLL=3.3V, VDD=1.2V, temperature=25℃ Process = Typical-Typical
Best case	VDDDLVD=3.63V, VDDPLVD=3.63V, VDDPLL=3.63V, VDD=1.32V temperature=0℃ Process = Fast-Fast
Best case (High temperature)	VDDDLVD=3.63V, VDDPLVD=3.63V, VDDPLL=3.63V, VDD=1.32V temperature=125℃ Process = Fast-Fast
Best case (Low temperature)	VDDDLVD=3.63V, VDDPLVD=3.63V, VDDPLL=3.63V, VDD=1.32V temperature=-40℃ Process = Fast-Fast
Worst case (High temperature)	VDDDLVD=2.97V, VDDPLVD=2.97V, VDDPLL=2.97V, VDD=1.08V temperature=125℃ Process =Slow-Slow
Worst Case (Low temperature)	VDDDLVD=2.97V, VDDPLVD=2.97V, VDDPLL=2.97V, VDD=1.08V temperature=-40℃ Process =Slow-Slow

LVDS Transmitter's timing is characterized with transmission line and measured at the receiver side. The test circuit and the three-state enable time's measure point are shows in the Figure22-3 and Figure22-4.

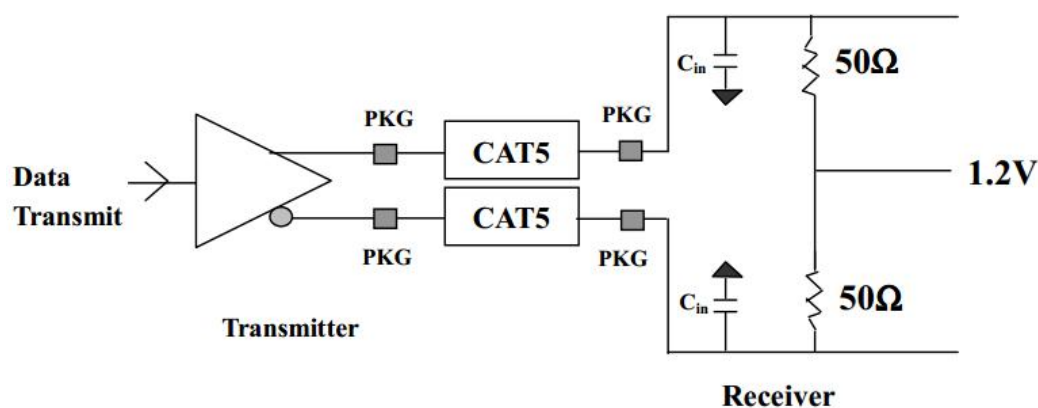


Fig. 9-3 Test Circuit of Three-state Enable Time

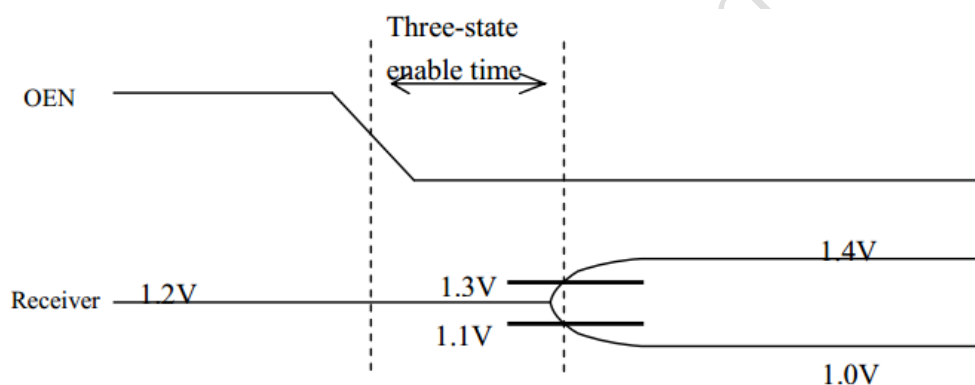


Fig. 9-4 Three-state Enable Time Measure Point

Table9-7 LVDS Transmitter AC Electrical Specifications

Symbol	Parameter	Conditions	Min	Typ	Max
Clock	Clock signal duty cycle	135MHz		57%	
t_{fall}	V_{od} fall time, 20~80%	$R_{load}=100\Omega\pm1\%$	260ps		$0.3 \cdot T_{ui\#}$
t_{rise}	V_{od} rise time, 20~80%	$R_{load}=100\Omega\pm1\%$	260ps		$0.3 \cdot T_{ui}$
T_{skew1}	$ t_{phla} - t_{plhb} $ or $ t_{phlb} - t_{plha} $, differential skew	$R_{load}=100\Omega\pm1\%$			50ps
$t_{TS\#}$	Data setup to CK_REF (135MHz)		2.1ns		
$t_{TH\#}$	Data hold from CK_REF (135MHz)		1.9ns		
$t_{TS\#}$	Data setup to CK_REF (85MHz)		2.7ns		
$t_{TH\#}$	Data hold from CK_REF (85MHz)		2.5ns		
$t_{TS\#}$	Data setup to CK_REF (20MHz)		8.2ns		
$t_{TH\#}$	Data hold from CK_REF (20MHz)		8ns		

9.4 Register description

Please refer to I2C chapter

9.5 Interface description

1.1.1 LVDS Transmitter Output

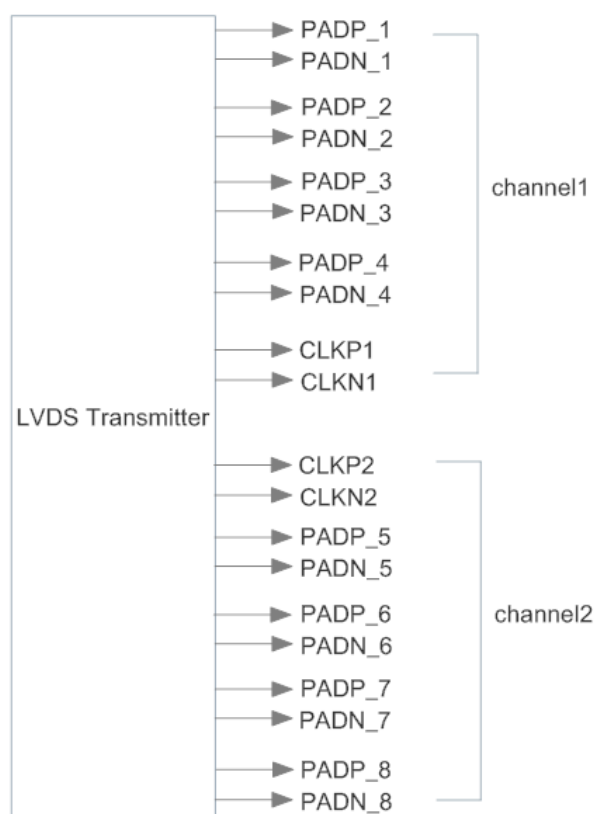


Fig. 9-5LVDS Transmitter Interface

When single channel mode, use channel1,channel2 output Z.

When dual channel mode,use channel1 and channel2.

1.1.2 LVTTTL Output

When LVDS works in LVTTTL mode, the LVDS output signals used as lcdc_data[19:0].

Table9-8LVDS Corresponding LCDC data in LVTTTL mode

LVDS output signals	lcdc_data
IO_LVDS_PADP_1	lcdc_data[0]
IO_LVDS_PADN_1	lcdc_data[1]
IO_LVDS_PADP_2	lcdc_data[2]
IO_LVDS_PADN_2	lcdc_data[3]
IO_LVDS_PADP_3	lcdc_data[4]
IO_LVDS_PADN_3	lcdc_data[5]
IO_LVDS_PADP_4	lcdc_data[6]
IO_LVDS_PADN_4	lcdc_data[7]
IO_LVDS_CLKP1	lcdc_data[8]
IO_LVDS_CLKN1	lcdc_data[9]
IO_LVDS_PADP_5	lcdc_data[10]
IO_LVDS_PADN_5	lcdc_data[11]
IO_LVDS_PADP_6	lcdc_data[12]
IO_LVDS_PADN_6	lcdc_data[13]
IO_LVDS_PADP_7	lcdc_data[14]
IO_LVDS_PADN_7	lcdc_data[15]
IO_LVDS_PADP_8	lcdc_data[16]
IO_LVDS_PADN_8	lcdc_data[17]
IO_LVDS_CLKP2	lcdc_data[18]
IO_LVDS_CLKN2	lcdc_data[19]

9.6 TimingDiagram

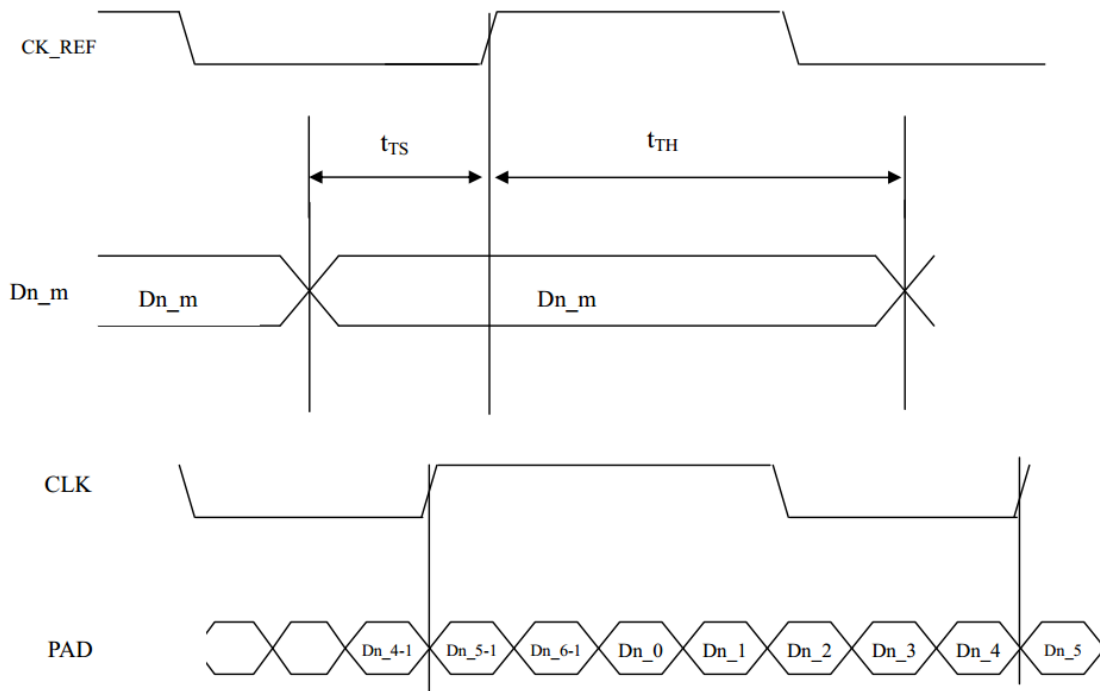


Fig. 9-6 Load and Shift Timing

9.7 Application Notes

When use dual channel lvds mode, the timing of LCDC must configure as below:

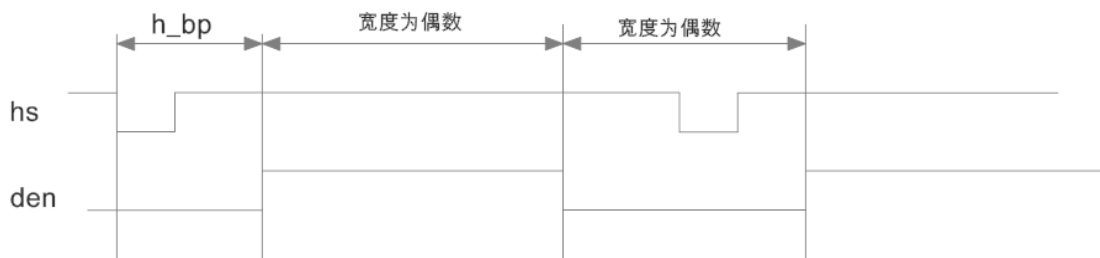


Fig. 9-7 LCDC Timing in Dual LVDS Mode

When h_{bp} is even, `lvds_con_start_phase` set to 0.

When h_{bp} is odd, `lvds_con_start_phase` set to 1.

The width of **den** must be even.

The width of **hs** must be even.

The **dclk** need invert to meet the timing of LVDS Transmitter.

Chapter 10 HDMI

10.1 Overview

HDMI TX is consisted of HDMI Transmitter Controller and HDMI Transmitter PHY which is fully compliant with HDMI 1.4a specification, supporting 3D Display and up to 4Kx2K highest HD display grade.

The HDMI TX provide functionality to transmit digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. HDMI TX can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. Content protection technology is available. HDMI TX offers a simple implementation for system on chip (SOC) for consumer electronics like DVD player/recorder and camcorder.

The HDMI TX is optimized for high speed (up to 3.4Gbps per TMDS link) High-Definition applications with robust timing and small silicon area in many process. HDMI TX contains controller and transmitter PHY circuit with programmable pre-emphasis, slew rate, output voltage swing and resistor values to drive transmit data with optimal signal quality and distance over the standard HDMI cable to a standard HDMI display device. The HDMI TX PHY contains all HDMI components including all I/O Library, high performance wide range PLL, the data symbol conversion/synchronization unit. The high performance drive and capture circuit is capable of working in the range of 250Mbps, 1.65Gbps, all the way up to 3.4Gbps in HDMI 1.4 standard per a TMDS pair.

The HDMI TX controller supports up to 300 MHz digital core design in many process, high definition multimedia interface (HDMI) v1.4a compliant transmitter. It supports all mandatory and optional 3D video formats defined in the HDMI specification 1.4a. HDTV formats up to 1080p with up to 48 bit deep color. With the inclusion of HDCP, the HDMI TX allows the secure transmission of protected content as specified by the HDCP v.1.2 protocol.

The HDMI TX helps reduce system design complexity and cost by incorporating such add on features as an I2C master for EDID reading, 5V tolerance on the I2C and hot plug detect pins, and CEC for high-level control functions between all of the various audiovisual products in a user's environment.

10.1.1 Features

- Very low power operation, less than 60mW in PHY during 1080P HD display
- HDMI 1.4/1.3/1.2/1.1, HDCP 1.2 and DVI 1.0 standard compliant transmitter
- Supports data rate from 25MHz, 1.65bps up to 3.4Gbps over a Single channel HDMI
- Support 3D function defined in HDMI 1.4 spec

- TMDS Tx Drivers with programmable output swing, resister values and pre-emphasis
- Supports all DTV resolutions including 480i/576i/480p/576p/720p/1080i/1080p
- Digital video interface supports a pixel size of 24, 30, 36, 48bits color depth in RGB
- S/PDIF output supports PCM, Dolby Digital, DTS digital audio transmission (32-192kHz Fs) using IEC60958 and IEC 61937
- Multiphase 4MHz fixed bandwidth PLL with low jitter
- DDC Bus I2C master interface at 3.3V
- HDCP encryption and decryption engine contains all the necessary logic to encrypt the incoming audio and video data
- Support HDMI LipSync if needed as addon feature
- Lower power operation with optimal power management feature
- Embedded ESD, scan support logic.
- The EDID and CEC function are also supported by HDMI Transmitter Controller
- Optional Monitor Detection supported through Hot Plug
- Optional HDMI controller solution available

10.2 Block Diagram

HDMI TX is consisted of HDMI Transmitter Controller and HDMI Transmitter PHY which is fully compliant with HDMI 1.4a specification.

The HDMI TX Controller use the different periods and encoding types to transmit audio, video, and control data types and packet definitions for audio and auxiliary data. The diagram shown below is the architecture of the HDMI TX.

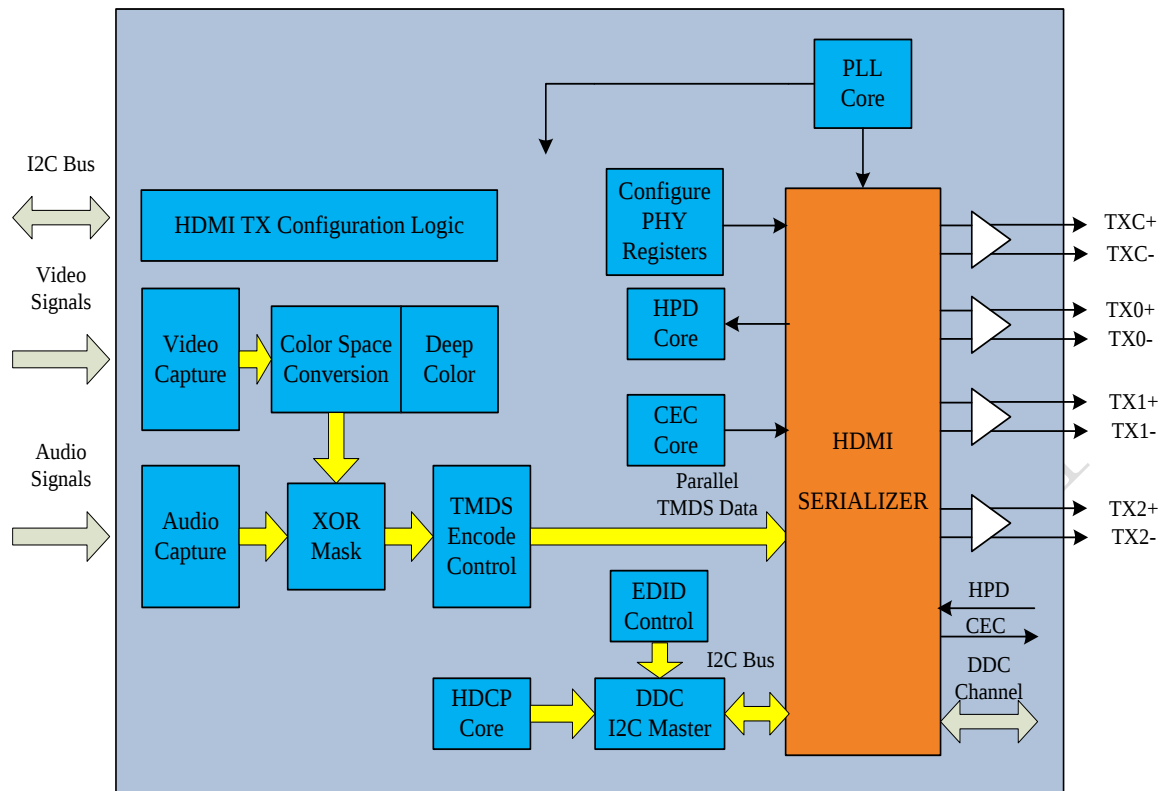


Fig. 10-1 HDMI Transmitter Architecture

10.3 Electrical Specification

HDMI Transmitter contains tunable source termination and pre-emphasis to enable high speed operation. The Transmitter meets the AC specifications below across all operating conditions specified. Rise and fall times are defined as the signal transition time between 20% and 80% of the nominal swing voltage (V_{swing}) of the device under test. The Transmitter intra-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1, between the true and complement signals of a given differential pair. This time difference is measured at the midpoint on the single-ended signal swing of the true and complement signals. The Transmitter inter-pair skew is the maximum allowable time difference (on both low-to-high and high-to-low transitions) as measured at TP1.

Normal Operating Conditions

Sym bol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{REF}	Reference Voltage	3.0	3.3	3.6	V
V_{CCN}	Supply Voltage Noise			100	mV _{p.p}
T_A	Ambient Temperature (with power applied)	0	25	70	°C

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
$V_{CC}^{1,2}$	Supply Voltage 3.3V	-0.3		4.0	V
$V_1^{1,2}$	Input Voltage	-0.3		$V_{CC}+0.3$	V
$V_0^{1,2}$	Output Voltage	-0.3		$V_{CC}+0.3$	V
$V_J^{1,2}$	Junction Temperature (with power applied)			125	°C

Transmitter DC Characteristics at TP1

Item	Value
Single-ended high level output voltage, V_H	$AV_{CC}-10mV < V_H < AV_{CC}+10mV$ when sink $\leq 165Mhz$ $AV_{CC}-200mV < V_H < AV_{CC}+10mV$ when sink $> 165Mhz$
Single-ended low level output voltage, V_L	$(AV_{CC} - 600mV) < V_L < (AV_{CC} - 400mV)$ when sink $\leq 165Mhz$ $(AV_{CC} - 700mV) < V_L < (AV_{CC} - 400mV)$ when sink $> 165Mhz$
Single-ended output swing voltage, V_{swing}	$400mV < V_{swing} < 600mV$
Single-ended standby (off) output voltage, V_{OFF}	$AV_{CC}+10mV$
Single-ended standby (off) output current, I_{OFF}	$ I_{OFF} < 10uA$

Transmitter AC Characteristics at TP1

Item	Value
Risetime/falltime (20%-80%)	$75psec < \text{Risetime/falltime} < 0.4 T_{bit}$
Overshoot, max	15% of full differential amplitude ($V_{swing} * 2$)
Undershoot, max	25% of full differential amplitude ($V_{swing} * 2$)
Intra-Pair Skew at Transmitter Connector, max	$0.15 T_{bit}$
Inter-Pair Skew at Transmitter Connector, max	$0.20 T_{pixel}$
TMDS Differential Clock Jitter, max	$0.25 T_{bit}$
Clock duty cycle	40% to 60%

Programmable Output Resistance and Output Equalization Level

Item	Value
Output Equalization level	10% to 60%
Termination Resistance	50ohm and 75 ohms selectable with fine steps
Output Swing Ranges	4 different levels

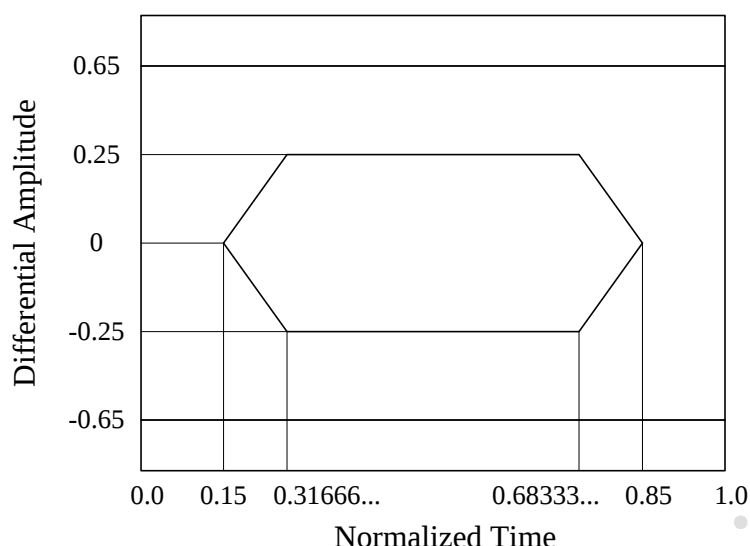


Fig. 10-2 The Eye Diagram of Differential TMDS Signals

The transmitter PHY will meet the above are the normalized eye diagram mask requirements at TP1 points for any data or clock TMDS output.

10.3.1 Control Signal – DDC

DDC (Display Data Channel) control signals follow the I2C Bus specifications. More details to be filled out from I2C specs.

Item	Value
High Voltage Level (Vih)	$-3.0V < V_{ih} < 3.8V$
Low Voltage Level (Vil)	$-0.5V < V_{il} < 1.5V$
SCL clock frequency	100KHz (max)
Rise time	$< 1000ns$
Fall time	$< 300ns$
Capacitive load on bus line	400pF

10.3.2 Control Signal – HPD

HPD (Hot Plug Detect) signal is used by the source to read the sink's E-DID. The sink needs to meet the following requirements for reliable detection.

For Sink

Item	Value
High Voltage Level (Vih)	$2.4V < V_{ih} < 5.3V$
Low Voltage Level (Vil)	$0V < V_{il} < 0.4V$

For Source

Item	Value
High Voltage Level (Voh)	$2.0V < V_{oh} < 5.3V$
Low Voltage Level (Vol)	$0V < V_{ol} < 0.8V$

10.4 HDMI Transmitter PHY

10.4.1 Description

The HDMI transmitter PHY is designed to be fully compatible with the HDMI 1.4 TP1 source characteristics. It is optimized for high speed (up to 3.4Gbps per

TMDS link) HD applications with robust timing, power consumption and small silicon area.

The transmitter PHY integrates low jitter PLL, bandgap reference and 4 TMDS channels to deliver multimedia data. Specialized transmitter driver circuit with tunable pre-emphasis, slew rate, and output voltage swing is able to transmit data with optimal signal quality and distance over the standard HDMI cable. Basically, the output driver switches the current supplied by the current source and drives the differential pair line.

10.4.2 Feature

1. Compatible with HDMI 1.4 specification
2. High speed, up to 3.4Gbps per channel throughput
3. Low power
4. Small size

10.4.3 Block Diagram

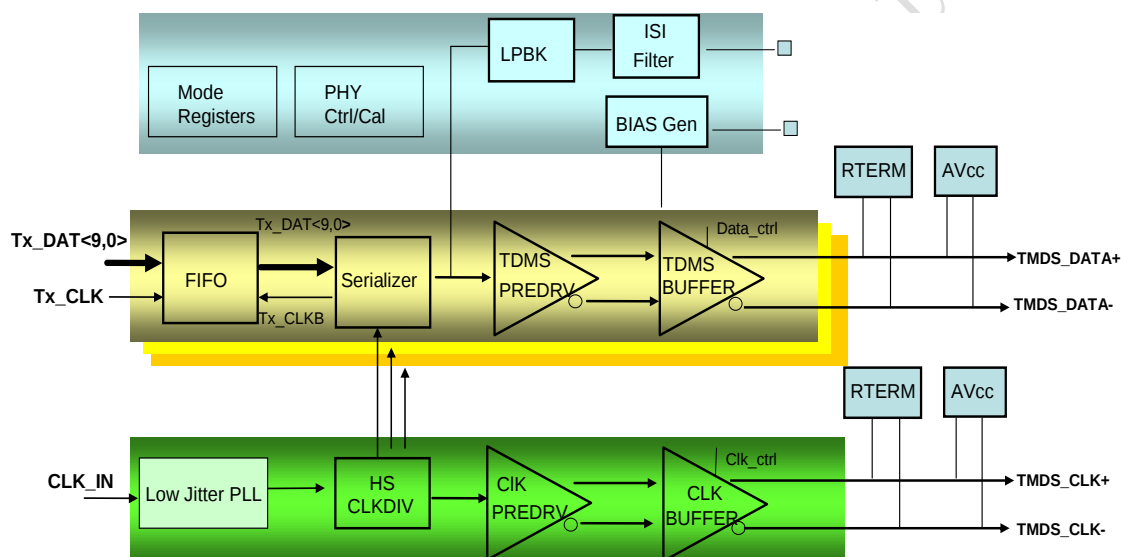


Fig. 10-3HDMI Transmitter PHY Block Diagram

10.4.4 HDMI Transmitter 1.4 PLL Description

The integrated PLL uses the pixel clock (recommended) or external crystal clock (optional) as the reference clock, and produce the digital core clock, the high frequency transmitting clock for the three data lane and the TMDS clock for the clock lane. In the PLL, Pre-divider is used for dividing the reference clock to the low frequency clock, and Post-divider is flexibly configured to support the difference video formats and color depths, such as 1080p with 1x 1.25x 1.5x and 2x color depth. The PLL has the variable bandwidth and it can keep the low jitter performance to comply with the jitter specification in the different configuration. The duty cycle of its output clock is 45% to 55%.

Note: The reference clock likes the pixel clock and crystal clock must meet the bellowing requirement.

Requirement Items	Value
-------------------	-------

Period clock Jitter - Peak to Peak	smaller than 100ps
Duty cycle	+/- 5%

The PLL of HDMI Transmitter provides a method as a low pass filter on the reference clock from pin_vclk on digital interface. The default bandwidth of PLL is 458 KHz.

The input jitter from the external reference clock to our HDMI PLL is mainly located in the low frequency bandwidth, for example below 1MHz. PLL loop to the jitter of reference clock has low pass effect, so we should use suitable PLL bandwidth design to eliminate the input jitter.

For example, the frequency of external reference clock is 148.5MHz.

Default set: N = 3, M = 30.

The output frequency is: $148.5\text{MHz} * \frac{30}{3} = 1.485\text{GHz}$.

The PLL bandwidth of default set is 458 KHz. There is the eliminating effect to the external reference clock jitter of 1MHz frequency. Under the condition of unchanging the frequency of external reference clock, we will gain stronger eliminating effect by setting the value of register referenced in Table 1-1 and Table 1-2.

Table 10-1 Some PHY Registers Description

ADDR	DEFAULT VALUE	DESCRIPTIONS
{ rege8 [0], rege7 [7:0]}	9'b00001111 0	Control the value of feedback dividing ratio, alias M ($16 \leq M \leq 512$)
reged [4:0]	5'b00011	Control the value of pre-dividing ratio, alias N ($1 \leq N \leq 15$)

Note: please refer to HDMI TX General Registers Description for more information.

Table 10-2 Configuration of Several Groups

Bandwidth	Frequency(MHz)	N/M
1.41MHz	148.5	2/20
458KHz	148.5	3/30
322.89KHz	148.5	6/60
229KHz	148.5	12/120

For example:

Set: N = 12, the value of **reged**[4:0] set 5'b01100;

M = 120, the value of {**rege8**[0], **rege7**[7:0]} set 9'b001111000.

The output frequency is: $148.5\text{MHz} * \frac{120}{12} = 1.485\text{GHz}$.

After modifying set, the PLL bandwidth is 229 KHz. To the external reference clock jitter, stronger eliminating effect exists.

So, just make sure: $\frac{M}{N} = 10$,

We can change PLL bandwidth under the condition of getting the same output frequency and test PLL performance the under condition of eliminating the jitter of external reference clock.

10.5 HDMI Transmitter Controller

The HDMI Transmitter Controller supports all the essential features of the newest HDMI Specification 1.4a. Various input video and audio format that can be captured by HDMI transmitter controller. The Video Capture support 24/30/36/48-bit RGB/YCbCr 4:4:4/4:2:2 separate/embedded syncs essential video formats and all mandatory and many optional 3D video formats. The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The HDCP1.2 is supported for protect the transmitted video and audio content which can be optioned by customer configure relative registers. The EDID and CEC function are also supported by HDMI Transmitter Controller. Customer can easily build the self-home theatre system with these features.

The following is the introduction of HDMI Transmitter Controller.

10.5.1 Description

The HDMI Transmitter Controller accommodate different periods and encoding types to transmit audio, video, and control data types and packet definitions for audio and auxiliary data. So, there are many important modules to implement above functions according to the HDMI Specification 1.4a. The Video Capture and Audio Capture modules are used to capture the various format data of video and audio for further process. The video data will be processed through the Color Space Conversion module or Deep Color module for high performance video data transmit, that function can be smartly configured with many relative registers. After the above process done, the video and audio data will be transform to standard format preparing for next step. The standard format video and audio will be encode to 10bits TMDS parallel data through TMDS Encode module for HDMI Transmitter PHY use. There are many other optional functions can be selected by customer according to their actual application. Likes the HDCP module is used for content protected. The EDID module is used for communication with HDMI Receiver, and the CEC module is used for customer control with one remote controller.

The following diagram is the Architecture of The HDMI Transmitter Controller.

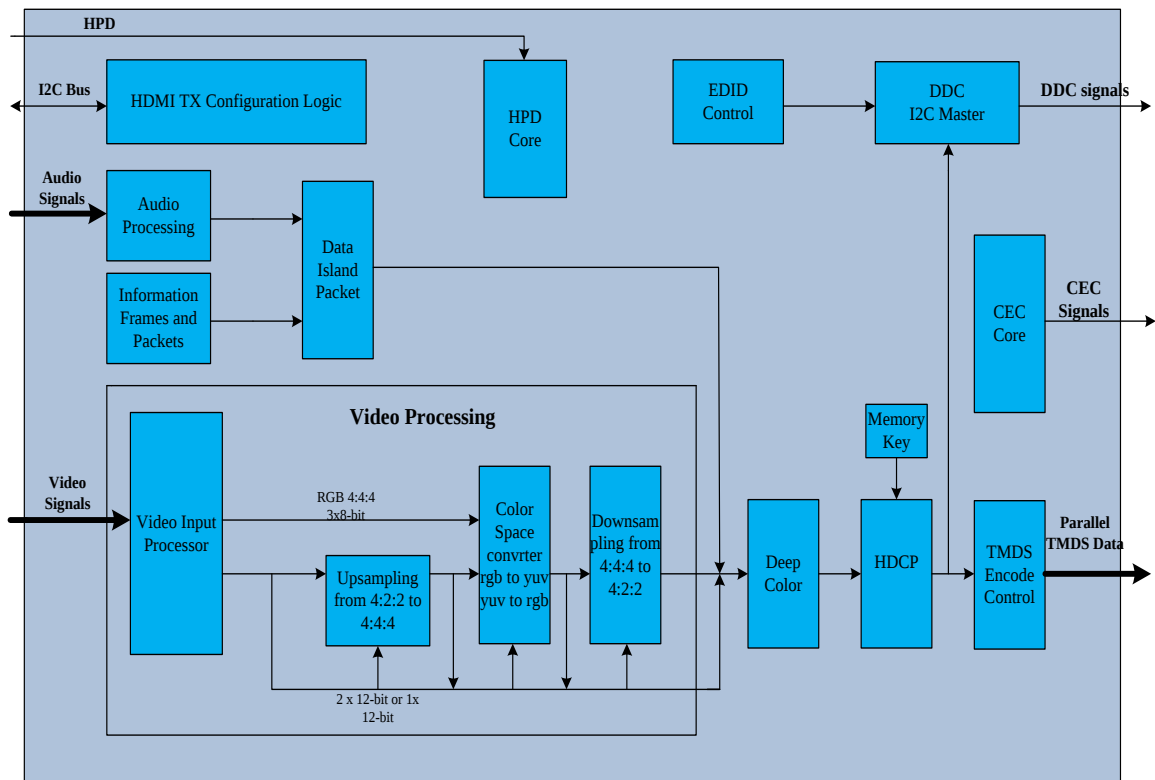


Fig. 10-4HDMI Transmitter Controller Block Diagram

10.5.2 Interface Timing

This sections showing below is the input and output timing relationship between the system and the HDMI TX controller.

Video Input Timing

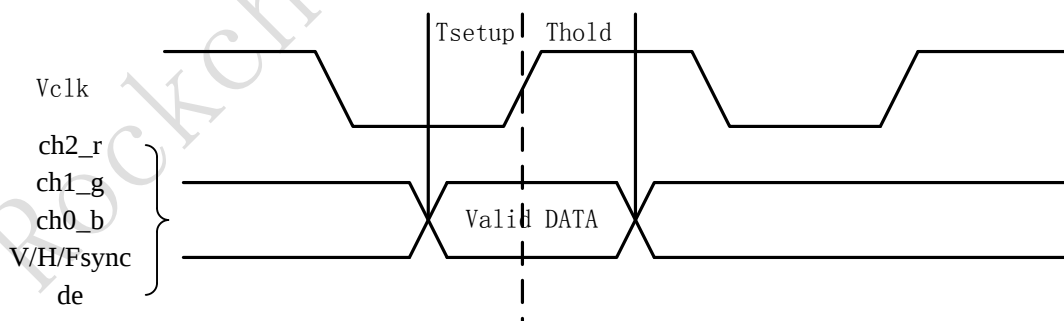


Fig. 10-5Video Input Timing

Table10-3Video Input Timing

SYMBOL	DESCRITITIONS	MIN	TYP	MAX	UNIT
Vclk	Vclk input period	6.67		40	ns
Vclk	Vclk input frequency	25		150	MHz
Vclk duty	Vclk input duty cycle	40	50	60	%

Tsetup	Setup time to Vclk positive edge	1.5			ns
Thold	Hold time to Vdclk positive edge	1			ns

SPDIF Audio

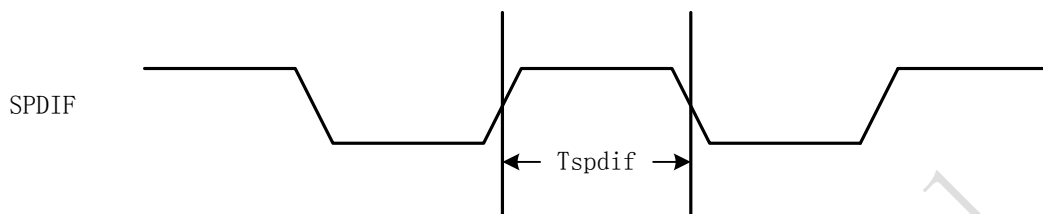


Fig. 10-6 SPDIF Input Timing

Table 10-4 SPDIF Input Timing

SYMBOL	DESCRIPTIONS	MIN	TYP	MAX	UNIT
Tspdif-sample	Sampling frequency	32		192	KHz
Tspdif	SPDIF cycle time		1		UI
Tspdifduty	SPDIF duty	90	100	110	%

I2S Audio

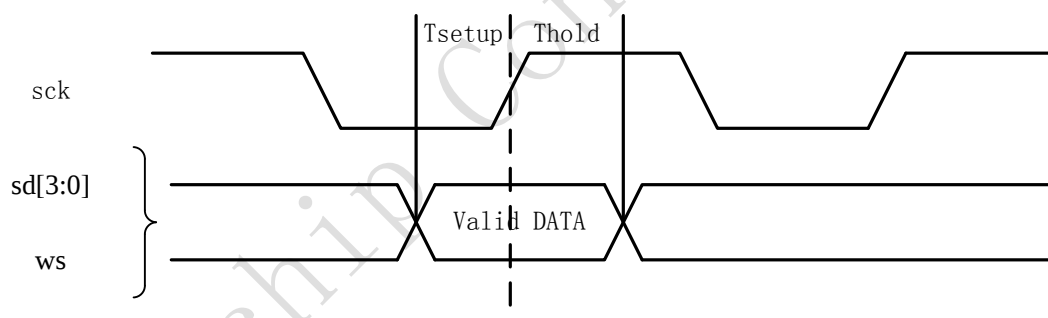


Fig. 10-7 I2S Input Timing

Table 10-5 I2S Input Timing

SYMBOL	DESCRIPTIONS	MIN	TYP	MAX	UNIT
Tsck-sample	Sampling frequency	32		192	KHz
Tsck	SCK cycle time		1		UI
Tsck-duty	SCK duty	90	100	110	%
Tsetup	Setup time to SCK rising edge	5			ns
Thold	Hold time from SCK rising edge	15			ns

10.5.3 Functional Description

The following section breaks the whole HDMI TX Controller into functional blocks such as Video Data Processing block, Audio Data Processing block, HDCP and EDID processing blocks, and so on. Each block has its own sub-modules. The focus is to describe each module functional and relative register setting. The

whole HDMI has many registers but most of them are needn't to change. This practically saves user a lot of time to configure the HDMI TX to their needs.

10.5.3.1 Video Data Processing Block

The video process contain video format timings, pixel encodings(RGB to YCbCr, or YCbCr to RGB), colorimetry and corresponding requirements. This function is implemented by some functional blocks, Video Capture block, Color Space Conversion block, and Deep Color block.

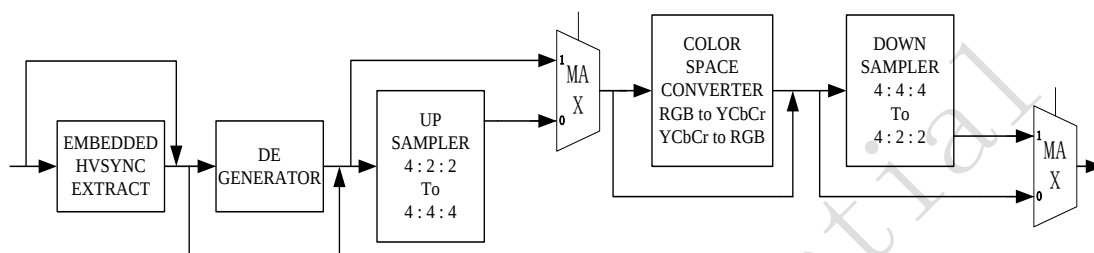


Fig. 10-8 Video Processing Module Diagram

The input video pixels can be encoded in either RGB, YCbCr 4:4:4 or YCbCr 4:2:2 formats by Color Space Conversion block.

The input Video data format is 24-bit. The deep color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate. HDMI Transmitter support video formats with TMDS rates below 25MHz (e.g. 13.5MHz for 480i/NTSC) that can be transmitted using a pixel-repetition scheme by setting relative registers.

The following interface timing diagram outlines the Video interface signal format. 24 bit data (we also support 36 bit data for deep color) in RGB can be captured by the rising edge of VCLK with 1ns setup time and 1ns hold time requirements. Control signals such as DE and VSync/HSync/FSync going with the same timing relationship.

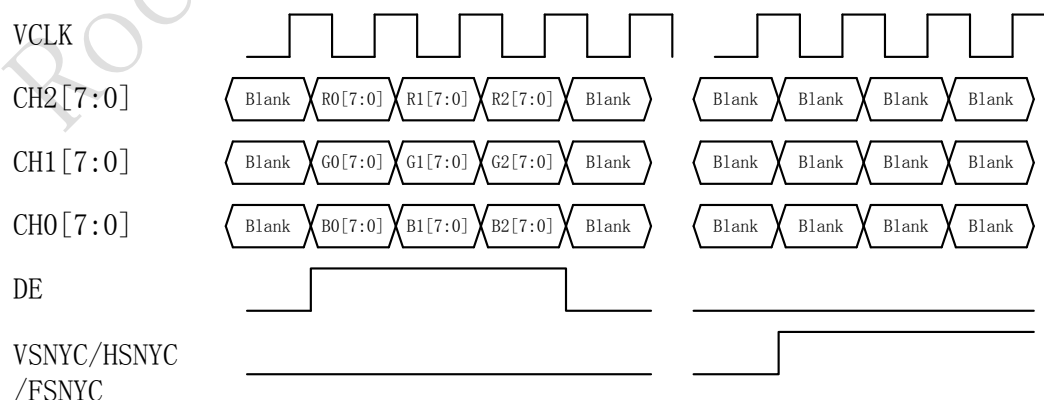


Fig. 10-9 Video Processing Timing

HDMI TX support input video data related format table is listed below.

Table10-6Video Data Related Format

Color Space	Pixel Encoding	Sync	Channel Width	Pin Nums
RGB	4:4:4	Separate	8	24
RGB	4:4:4	Separate	10	30
RGB	4:4:4	Separate	12	36
YCbCr	4:4:4	Separate	8	24
YCbCr	4:4:4	Separate	10	30
YCbCr	4:4:4	Separate	12	36
YCbCr	4:2:2	Separate	8	16
YCbCr	4:2:2	Separate	10	20
YCbCr	4:2:2	Separate	12	24
YCbCr	4:4:4	Embedded	8	24
YCbCr	4:4:4	Embedded	10	30
YCbCr	4:4:4	Embedded	12	36
YCbCr	4:2:2	Embedded	8	16
YCbCr	4:2:2	Embedded	10	20
YCbCr	4:2:2	Embedded	12	24

Embedded SYNC Extraction module

The module is used to extract Vsync and Hsync signals from input video data stream such as ITU656 format. With setting the relative registers, this functional module can extract correct video sync signals for later process block using.

Data Enable(DE) Generator

HDMI Transmitter has DE signal generator by incoming HSYNCs, VSYNCs and Video clock. External DE is optional and selected by appropriate register settings. This feature is particularly useful when interfacing to MPEG decoders that do not provide a specific DE output signal.

Color Space Conversion

HDMI Transmitter Color space conversion (CSC) is available to interface for several MPEG decoders like with YCbCr-only outputs, and to provide full DVI backwards compatibility.

The function of this module is to perform color space conversion functionality as listed below.

1. Convert RGB input Video data to YCbCr Video data.
2. Convert YCbCr input Video data to RGB Video data.
3. upsample for YCbCr 4:2:2 to YCbCr 4:4:4
4. downsample for YCbCr 4:4:4 to YCbCr 4:2:2

Deep Color function

The input Video data can have a pixel size of 24, 30, 36 or 48 bits. The deep color block is used to deal with different pixel size. Video at the default 24-bit color depth is carried at a TMDS clock rate equal to the pixel clock rate. Higher color depths are carried using a correspondingly higher TMDS clock rate.

Video Bist mode

HDMI Transmitter Controller can provide a BIST mode for display testing or other use. There are three mode can be choose. Increase data color bar mode, normal color bar mode, mute mode (black on the screen).

10.5.3.2 Audio Data Processing Block

The HDMI TX audio process contain audio clock regeneration, placement of audio samples within packets, packet timing control, audio sample rates setting, and channel/speaker assignments. This function is implemented by Audio Capture blocks

The Audio Capture support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz.

The scheme of audio processing as shown in the figure below.

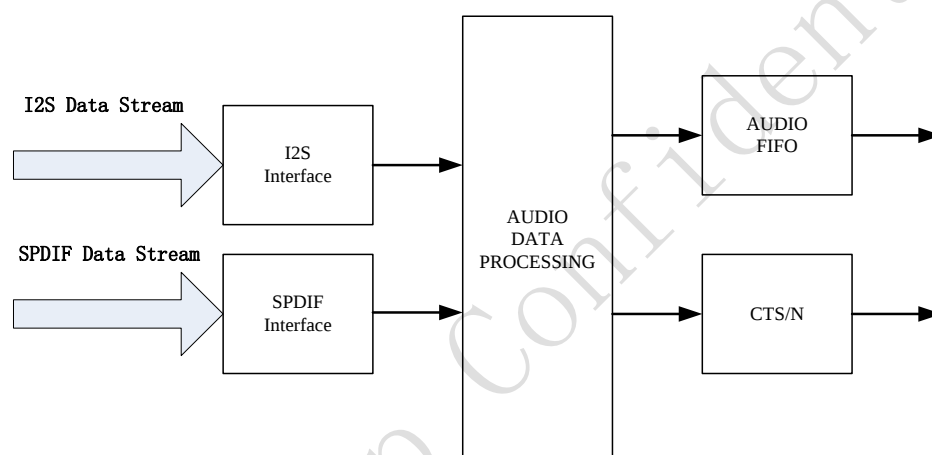


Fig. 10-10 Audio Data Processing Block Diagram

I2S Interface

The function of this module is to implement I2S audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. Four I2S inputs also allow transmission of DVD-Audio and decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports from 2-channel to 8-channel audio up to 192 kHz. The I2S pins must also be coherent with mclk. The appropriate registers must be configured to describe the format of audio being input. This information is passed over the HDMI link in the CEA-861D Audio Info (AI) packets. Table shows the I2S 8 channel audio formats that are supported for each of the video formats.

Table10-7 I2S 2 Channel Audio Sampling Frequency at Each Video Format

Video Format	32 KHz	44.1 KHz	48 KHz	88.2 KHz	96 KHz	176.4 KHz	192 KHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1440x480i/1440x576i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table10-8I2S 8 Channel Audio Sampling Frequency at Each Video Format

Video Format	32 KHz	44.1 KHz	48 KHz	88.2 KHz	96 KHz	176.4 KHz	192 KHz
720x480p /720x576p	Yes	Yes	Yes	No	No	No	No
1440x480i/1440x576i	Yes	Yes	Yes	Yes	No	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

SPDIF Interface

The function of this module is to implement SPDIF audio input feature. The incoming audio stream is captured, processed then transmitted into the TMDS link. SPDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI specification. SPDIF input supports audio sampling rates from 32 to 192 KHz. The following shows the SPDIF audio formats that are supported for each of the video formats

Table10-9SPDIF Sampling Frequency at Each Video Format

Video Format	32 KHz	44.1 KHz	48 KHz	88.2 KHz	96 KHz	176.4 KHz	192 KHz
720x480p /720x576p	Yes	Yes	Yes	Yes	Yes	No	No
1440x480i/1440x576i	Yes	Yes	Yes	Yes	Yes	No	No
720p	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080i	Yes	Yes	Yes	Yes	Yes	Yes	Yes
1080p	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Audio Sample Clock Capture and Regeneration

Audio data being carried across the HDMI link, which is driven by a TMDS clock running at a rate corresponding to the video pixel rate, does not retain the original audio sample clock. The task of recreating this clock at the Sink is called Audio Clock Regeneration.

The HDMI Transmitter determine the fractional relationship between the TMDS clock and an audio reference clock (128 audio sample rate [fs]) and pass the numerator and denominator of that fraction to the HDMI Sink across the HDMI link. The Sink then re-create the audio clock from the TMDS clock by using a clock divider and a clock multiplier.

The exact relationship between the two clocks will be.

$$128 \cdot f_S = f_{\text{TMDS_clock}} \cdot N / \text{CTS}.$$

The scheme of the Audio Sample Clock Capture and Regeneration as shown below

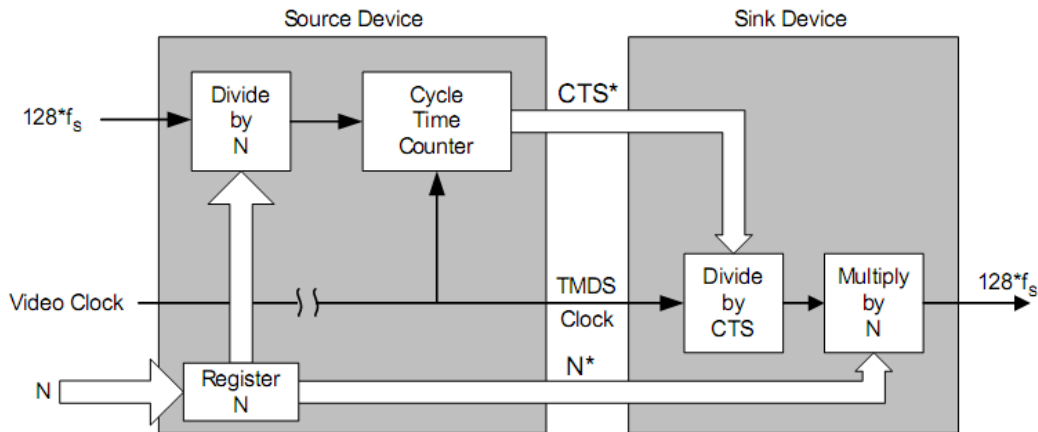


Fig. 10-11 Audio Clock Regeneration Model

10.5.3.3 DDC

The DDC functional block is used for configuration and status exchange between the HDMI Source and HDMI Sink. HDMI Transmitter Controller has I2C Master Interface for DDC transactions. It enables for host controller to read EDID, HDCP authentication by issuing simple register access. The I2C bus speed is limited by DDC specification. DDC bus access frequency can be controlled.

10.5.3.4 EDID

Extended Display Identification Data (EDID) was created by VESA to enable plug and play capabilities of monitors. This data, which is stored in the sink device, describes video formats that the DTV Monitor is capable of receiving and rendering. The information is supplied to the source device, over the interface, upon the request of the source device. The source device then chooses its output format, taking into account the format of the original video stream and the formats supported by the DTV Monitor. The function of this module is to implement EDID feature.

10.5.3.5 HDCP

HDMI Transmitter has a capability for HDCP authentication by hardware. The function of this module is to implement HDCP encryption feature. This feature can be turned on or off depending on register setting.

10.5.3.6 Hot Plug Detect

HDMI Transmitter has a capability for detecting the Sink plug in or plug out, and launch an interrupt and registers state indicating for software controlling.

10.5.3.7 TMDS Encoder

The TMDS encoder converts the 2/4/8 bits data into the 10 bit DC-balanced TMDS data.

HDMI TX put the TMDS encoding on the audio /video /aux data received from the HDCP XOR mask. This data is output onto three TMDS differential data lines along with a TMDS differential clock.

10.5.3.8 CEC

The CEC functional block provides high-level control functions between all of the various audiovisual products in a user's environment through one line.

10.5.3.9 Optional Lipsync

HDMI sinks and repeaters can now declare audio/video latency information in their EDIDs. HDMI TX can read the audio/video latency information from HDMI sinks, than it may delay audio or video to compensate for latencies in downstream devices.

10.6 Register Description

The tables showing below are the HDMI TX general registers description. User can use HDMI TX smartly by configuring these registers.

10.6.1 Register Summary

Name	Offset	Size	Reset Value	Description
HDMI_reg00	0x0000	B	0x67	Register00
HDMI_reg01	0x0004	B	0x01	Register01
HDMI_reg02	0x0008	B	0x30	Register02
HDMI_reg04	0x0010	B	0x08	Register04
HDMI_reg05	0x0014	B	0x00	Register05
HDMI_reg08	0x0020	B	0x00	Register08
HDMI_reg09	0x0024	B	0x00	Register09
HDMI_reg0a	0x0028	B	0x00	Register0a
HDMI_reg0b	0x002c	B	0x00	Register0b
HDMI_reg0c	0x0030	B	0x00	Register0c
HDMI_reg0d	0x0034	B	0x00	Register0d
HDMI_reg0e	0x0038	B	0x00	Register0e
HDMI_reg0f	0x003c	B	0x00	Register0f
HDMI_reg10	0x0040	B	0x00	Register10
HDMI_reg11	0x0044	B	0x00	Register11
HDMI_reg12	0x0048	B	0x00	Register12
HDMI_reg13	0x004c	B	0x00	Register13
HDMI_reg14	0x0050	B	0x00	Register14
HDMI_reg15	0x0054	B	0x00	Register15
HDMI_reg30	0x00c0	B	0x00	Register30

Name	Offset	Size	Reset Value	Description
HDMI_reg31	0x00c4	B	0x00	Register31
HDMI_reg32	0x00c8	B	0x00	Register32
HDMI_reg33	0x00cc	B	0x00	Register33
HDMI_reg34	0x00d0	B	0x00	Register34
HDMI_reg35	0x00d4	B	0x01	Register35
HDMI_reg37	0x00dc	B	0x00	Register37
HDMI_reg38	0x00e0	B	0x3c	Register38
HDMI_reg39	0x00e4	B	0x00	Register39
HDMI_reg3a	0x00e8	B	0x00	Register3a
HDMI_reg3f	0x00fc	B	0x00	Register3f
HDMI_reg40	0x0100	B	0x18	Register40
HDMI_reg41	0x0104	B	0x00	Register41
HDMI_reg4a	0x0128	B	0x00	Register4a
HDMI_reg4b	0x012c	B	0x40	Register4b
HDMI_reg4c	0x0130	B	0x00	Register4c
HDMI_reg4d	0x0134	B	0x00	Register4d
HDMI_reg4e	0x0138	B	0x00	Register4e
HDMI_reg4f	0x013c	B	0x00	Register4f
HDMI_reg50	0x0140	B	0x00	Register50
HDMI_reg52	0x0148	B	0x12	Register52
HDMI_reg53	0x014c	B	0x04	Register53
HDMI_reg57	0x015c	B	0x20	Register57
HDMI_reg58	0x0160	B	0x00	Register58
HDMI_reg63	0x018c	B	0x26	Register63
HDMI_reg64	0x0190	B	0x2c	Register64
HDMI_reg65	0x0194	B	0x00	Register65
HDMI_reg6c	0x01b0	B	0x00	Register6c
HDMI_reg7b	0x01ec	B	0x00	Register7b
HDMI_reg7c	0x01f0	B	0x00	Register7c
HDMI_reg7d	0x01f4	B	0x00	Register7d
HDMI_reg7e	0x01f8	B	0x00	Register7e
HDMI_reg7f	0x01fc	B	0x00	Register7f
HDMI_reg80	0x0200	B	0x00	Register80
HDMI_reg81	0x0204	B	0x00	Register81
HDMI_reg82	0x0208	B	0x00	Register82
HDMI_reg95	0x0254	B	0x00	Register95
HDMI_reg96	0x0258	B	0x00	Register96
HDMI_reg97	0x025c	B	0x00	Register97
HDMI_reg98	0x0260	B	0x03	Register98
HDMI_reg9c	0x0270	B	0x00	Register9c

Name	Offset	Size	Reset Value	Description
HDMI_reg9e	0x0278	B	0x01	Register9e
HDMI_reg9f	0x027c	B	0x00	Register9f
HDMI_rega0	0x0280	B	0x00	Registera0
HDMI_rega1	0x0284	B	0x00	Registera1
HDMI_rega2	0x0288	B	0x00	Registera2
HDMI_rega3	0x028c	B	0x00	Registera3
HDMI_rega4	0x0290	B	0x00	Registera4
HDMI_rega5	0x0294	B	0x00	Registera5
HDMI_rega6	0x0298	B	0x00	Registera6
HDMI_rega7	0x029c	B	0x00	Registera7
HDMI_rega8	0x02a0	B	0x00	Registera8
HDMI_rega9	0x02a4	B	0x00	Registera9
HDMI_regaa	0x02a8	B	0x00	Registeraa
HDMI_regab	0x02ac	B	0x00	Registerab
HDMI_regac	0x02b0	B	0x00	Registerac
HDMI_regad	0x02b4	B	0x00	Registerad
HDMI_regae	0x02b8	B	0x00	Registerae
HDMI_regaf	0x02bc	B	0x00	Registeraf
HDMI_regb0	0x02c0	B	0x00	Registerb0
HDMI_regb1	0x02c4	B	0x00	Registerb1
HDMI_regb2	0x02c8	B	0x00	Registerb2
HDMI_regb3	0x02cc	B	0x00	Registerb3
HDMI_regb4	0x02d0	B	0x00	Registerb4
HDMI_regb5	0x02d4	B	0x00	Registerb5
HDMI_regb6	0x02d8	B	0x00	Registerb6
HDMI_regb7	0x02dc	B	0x00	Registerb7
HDMI_regb8	0x02e0	B	0x00	Registerb8
HDMI_regb9	0x02e4	B	0x00	Registerb9
HDMI_regba	0x02e8	B	0x00	Registerba
HDMI_regbb	0x02ec	B	0x00	Registerbb
HDMI_regbc	0x02f0	B	0x00	Registerbc
HDMI_regbd	0x02f4	B	0x00	Registerbd
HDMI_regbe	0x02f8	B	0x00	Registerbe
HDMI_regc0	0x0300	B	0xc0	Registerc0
HDMI_regc1	0x0304	B	0x00	Registerc1
HDMI_regc2	0x0308	B	0x78	Registerc2
HDMI_regc3	0x030c	B	0x00	Registerc3
HDMI_regc4	0x0310	B	0x00	Registerc4
HDMI_regc5	0x0314	B	0x00	Registerc5
HDMI_regc8	0x0320	B	0x00	Registerc8

Name	Offset	Size	Reset Value	Description
HDMI_regc9	0x0324	B	0x50	Registerc9
HDMI_regce	0x0338	B	0x01	Registerce
HDMI_regd0	0x0340	B	0x00	Registerd0
HDMI_regd1	0x0344	B	0x00	Registerd1
HDMI_regd2	0x0348	B	0x00	Registerd2
HDMI_regd3	0x034c	B	0x00	Registerd3
HDMI_regd4	0x0350	B	0x03	Registerd4
HDMI_regd5	0x0354	B	0x09	Registerd5
HDMI_regd6	0x0358	B	0x03	Registerd6
HDMI_regd7	0x035c	B	0x00	Registered7
HDMI_regd8	0x0360	B	0xff	Registerd8
HDMI_regd9	0x0364	B	0xff	Registerd9
HDMI_regda	0x0368	B	0x00	Registerda
HDMI_regdb	0x036c	B	0x00	Registerdb
HDMI_regdc	0x0370	B	0xd0	Registerdc
HDMI_regdd	0x0374	B	0x20	Registerdd
HDMI_regde	0x0378	B	0x00	Registerde
HDMI_rege0	0x0380	B	0x23	Registere0
HDMI_rege1	0x0384	B	0x0f	Registere1
HDMI_rege2	0x0388	B	0xaa	Registere2
HDMI_rege3	0x038c	B	0x0f	Registere3
HDMI_rege7	0x039c	B	0x1e	Registere7
HDMI_rege8	0x03a0	B	0x00	Registere8
HDMI_reged	0x03b4	B	0x03	Registered

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

10.6.2 Detail Register Description

HDMI_reg00

Address: Operational Base + offset (0x0400)

Register00

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6	RW	0x1	sw_reset_ana Soft reset for analog part 0: reset 1: not

Bit	Attr	Reset Value	Description
5	RW	0x1	sw_reset_dig Soft reset for digital part 0: reset 1: not
4	RW	0x0	cfg_clk_inv Register Configuration clock invert 0: not invert 1: invert
3	RW	0x0	vclk_inv Vclk invert select 0: not invert 1: invert
2	RW	0x1	cfg_clk_switch Registers configuration clock switch 0 : use TMDs clock from analog PHY 1 : use system clock
1	RW	0x1	pd_dig System power down for digital function 0 : not 1 : power down
0	RW	0x1	interrupt_polarity Interrupt polarity 1 : Active High 0 : Active low

HDMI_reg01

Address: Operational Base + offset (0x0404)

Register01

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved

Bit	Attr	Reset Value	Description
3:1	RW	0x0	input_video_fmt Input video format 000: RGB and YCbCr 4:4:4 101: DDR RGB 4:4:4 or YCbCr 4:4:4 110: DDR YCbCr 4:2:2
0	RW	0x1	de_sel DE select 0: internal DE 1: external DE

HDMI_reg02

Address: Operational Base + offset (0x0408)

Register02

Bit	Attr	Reset Value	Description
7:6	RW	0x0	video_output_fmt Video output format 00: RGB 4:4:4 01: YCbCr 4:4:4 10: YCbCr 4:2:2
5:4	RW	0x3	data_width_422 Data width for 4:2:2 input 00: 12 bits 01: 10 bits 11: 8 bits
3:0	RW	0x0	reserved

HDMI_reg04

Address: Operational Base + offset (0x0410)

Register04

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x1	sof_sel After 1st SOF(the first edge of the Vsync) for external DE sample 0: after SOF 1: Not
2:1	RW	0x0	reserved
0	RW	0x0	csc_en CSC (Color Space Convert) enable. This function need additional license from Innosilicon. 0: no CSC 1: enable CSC

HDMI_reg05

Address: Operational Base + offset (0x0414)

Register05

Bit	Attr	Reset Value	Description
7	RW	0x0	clear_avmute Clear avmute
6	RW	0x0	set_avmute Set avmute
5:2	RW	0x0	reserved
1	RW	0x0	audio_mute Audio mute
0	RW	0x0	video_black Video black

HDMI_reg08

Address: Operational Base + offset (0x0420)

Register08

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x0	vs_polarity VSYNC polarity 0 : Negative 1 : Positive
2	RW	0x0	hs_polarity HSYNC polarity 0 : Negative 1 : Positive
1	RW	0x0	interlace_progressiv_sel Interlace/Progressive 0 : Progressive 1 : Interlace
0	RW	0x0	ext_video_para_set_en External video parameter setting enable 0 : disable 1 : enable

HDMI_reg09

Address: Operational Base + offset (0x0424)

Register09

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_total_part1 External horizontal total part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0a

Address: Operational Base + offset (0x0428)

Register0a

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	ext_hs_total_part2 External horizontal total part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0b

Address: Operational Base + offset (0x042c)

Register0b

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_blank_part1 External horizontal blank part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0c

Address: Operational Base + offset (0x0430)

Register0c

Bit	Attr	Reset Value	Description
7:3	RW	0x0	reserved
2:0	RW	0x0	ext_hs_blank_part2 External horizontal blank part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0d

Address: Operational Base + offset (0x0434)

Register0d

Bit	Attr	Reset Value	Description
7:0	RW	0x00	Ext_hs_delay_part1 External horizontal delay part1. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0e

Address: Operational Base + offset (0x0438)

Register0e

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1:0	RW	0x0	Ext_hs_delay_part2 External horizontal delay part2. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg0f

Address: Operational Base + offset (0x043c)

Register0f

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_hs_sync_part1 External horizontal duration part1. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg10

Address: Operational Base + offset (0x0440)

Register10

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1:0	RW	0x0	ext_hs_sync_part2 External horizontal duration part2. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg11

Address: Operational Base + offset (0x0444)

Register11

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ext_vertical_total_part1 External vertical total part1. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg12

Address: Operational Base + offset (0x0448)

Register12

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	ext_vertical_total_part2 External vertical total part2. It is not need to be set at normal resolution. Just for special resolution or test purpose

HDMI_reg13

Address: Operational Base + offset (0x044c)

Register13

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	ext_vertical_blank External vertical blank. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg14

Address: Operational Base + offset (0x0450)

Register14

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	ext_vertical_dly External vertical delay. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg15

Address: Operational Base + offset (0x0454)

Register15

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved

Bit	Attr	Reset Value	Description
5:0	RW	0x00	ext_vertical_duration External vertical duration. It is not need to be set at normal resolution. Just for special resolution or test purpose.

HDMI_reg30

Address: Operational Base + offset (0x04c0)

Register30

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hs_place_at_itu656_part1 HSYNC placement at ITU656.

HDMI_reg31

Address: Operational Base + offset (0x04c4)

Register31

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hs_place_at_itu656_part2 HSYNC placement at ITU656.

HDMI_reg32

Address: Operational Base + offset (0x04c8)

Register32

Bit	Attr	Reset Value	Description
7:0	RW	0x00	vs_place_at_itu656_part1 VSYNC placement at ITU656.

HDMI_reg33

Address: Operational Base + offset (0x04cc)

Register33

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:0	RW	0x00	vs_place_at_itu656_part2 VSYNC placement at ITU656.

HDMI_reg34

Address: Operational Base + offset (0x04d0)

Register34

Bit	Attr	Reset Value	Description
7	RW	0x0	sync_place_en SYNC placement at ITU656 enable
6:0	RW	0x0	reserved

HDMI_reg35

Address: Operational Base + offset (0x04d4)

Register35

Bit	Attr	Reset Value	Description
7	RW	0x0	cts__sel CTS source select 0: internal CTS 1: external CTS
6:5	RW	0x0	downsample_sel Downsampling select 00b: No downsampling 01b: 1/2 downsampling 10b: 1/4 down sampling
4:3	RW	0x0	audio_type_sel Audio type select 00b: I2S 01b: S/PDIF
2	RW	0x0	mclk_sel MCLK select
1:0	RW	0x1	mclk_ratio MCLK ratio 00 : 128 fs 01 : 256 fs 10 : 384 fs 11 : 512 fs

HDMI_reg37

Address: Operational Base + offset (0x04dc)

Register37

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	sample_freq_sel Sampling frequency for I2S audio 0011: 32 kHz 0000: 44.1 kHz 0010: 48 kHz 1000: 88.2 kHz 1010: 96 kHz 1100: 176.4 kHz 1110: 192 kHz

HDMI_reg38

Address: Operational Base + offset (0x04e0)

Register38

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved
5:2	RW	0xf	i2s_sel I2S enable for the four I2S pins 0001: I2S0 0010: I2S1 0100: I2S2 1000: I2S3
1:0	RW	0x0	i2s_fmt I2S format 00: standard I2S mode 01: right-justified I2S mode 10: left-justified I2S mode

HDMI_reg39

Address: Operational Base + offset (0x04e4)

Register39

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:6	RW	0x0	audio_channel3_input_sel Audio channel3 input 2'b00 : I2S3 2'b01 : I2S2 2'b10 : I2S1 2'b11 : I2S0
5:4	RW	0x0	audio_channel2_input_sel Audio channel2 input 2'b00 : I2S2 2'b01 : I2S1 2'b10 : I2S0 2'b11 : I2S3
3:2	RW	0x0	audio_channel1_input_sel Audio channel1 input 2'b00 : I2S1 2'b01 : I2S0 2'b10 : I2S3 2'b11 : I2S2
1:0	RW	0x0	audio_channel0_input_sel Audio channel0 input 2'b00 : I2S0 2'b01 : I2S3 2'b10 : I2S2 2'b11 : I2S1

HDMI_reg3a

Address: Operational Base + offset (0x04e8)

Register3a

Bit	Attr	Reset Value	Description
7	RW	0x0	lr_swap_ch7_8 Left/Right data swap for ch7/8
6	RW	0x0	lr_swap_ch5_6 Left/Right data swap for ch5/6

Bit	Attr	Reset Value	Description
5	RW	0x0	lr_swap_ch3_4 Left/Right data swap for ch3/4
4	RW	0x0	lr_swap_ch1_2 Left/Right data swap for ch1/2
3:0	RW	0x0	spdif_sample_freq S/PDIF sampling frequency 0011: 32 kHz. 0000: 44.1 kHz. 0010: 48 kHz. 1000: 88.2 kHz. 1010: 96 kHz. 1100: 176.4 kHz. 1110: 192 kHz.

HDMI_reg3f

Address: Operational Base + offset (0x04fc)

Register3f

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	ncts_part1 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg40

Address: Operational Base + offset (0x0500)

Register40

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x18	ncts_part2 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg41

Address: Operational Base + offset (0x0504)

Register41

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ncts_part3 20-bit N-CTS Value for audio clock generation at Sink end. N-CTS=reg3f[3:0],reg40[7:0],reg41[7:0] Use this function please refer to the HDMI specification at "Recommended N and Expected CTS Values"

HDMI_reg4a

Address: Operational Base + offset (0x0528)

Register4a

Bit	Attr	Reset Value	Description
7:2	RW	0x0	reserved
1	RO	0x0	ddc_sda_bus_statue DDC SDA bus status
0	RO	0x0	ddc_scl_bus_statue DDC SCL bus status

HDMI_reg4b

Address: Operational Base + offset (0x052c)

Register4b

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x40	ddc_bus_access_freq_lsb DDC bus access frequency (LSB)

HDMI_reg4c

Address: Operational Base + offset (0x0530)

Register4c

Bit	Attr	Reset Value	Description
7:0	RW	0x00	ddc_bus_access_freq_msb DDC bus access frequency (MSB)

HDMI_reg4d

Address: Operational Base + offset (0x0534)

Register4d

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_segment_pointer EDID segment pointer

HDMI_reg4e

Address: Operational Base + offset (0x0538)

Register4e

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_word_addr EDID word address

HDMI_reg4f

Address: Operational Base + offset (0x053c)

Register4f

Bit	Attr	Reset Value	Description
7:0	RW	0x00	edid_fifo_rd_addr EDID FIFO read address

HDMI_reg50

Address: Operational Base + offset (0x0540)

Register50

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RO	0x00	edid_rd_access_window EDID reading access window

HDMI_reg52

Address: Operational Base + offset (0x0548)

Register52

Bit	Attr	Reset Value	Description
7	RW	0x0	authentication_start Authentication start
6	RW	0x0	bksv_not_in_blacklist BKSV is not in the blacklist
5	RW	0x0	bksv_in_blacklist BKSV is in the blacklist
4	RW	0x1	encpte_en current frame encrypted en 0: current frame should not be encrypted 1: current frame should be encrypted
3	RW	0x0	authentication_stop Authentication Stop
2	RW	0x0	advanced_mode_sel 0: do not use advanced cipher mode 1: use advanced cipher mode
1	RW	0x1	mode_sel mode selection 0: DVI mode 1: HDMI mode
0	RW	0x0	hdcp_reset HDCP reset

HDMI_reg53

Address: Operational Base + offset (0x054c)

Register53

Bit	Attr	Reset Value	Description
7	RW	0x0	disable_127_chk Disable 127 check
6	RW	0x0	skip_bksv_blacklist_chk Skip BKSv blacklist check
5	RW	0x0	pj_chk_en Enable Pj check
4	RW	0x0	disable_dev_num_check Disable device number check
3	RW	0x0	dly_ri_chk Delay Ri check by one clock
2	RW	0x1	use_preset Use preset An value
1:0	RW	0x0	key_comb Key combination

HDMI_reg57

Address: Operational Base + offset (0x055c)

Register57

Bit	Attr	Reset Value	Description
7	RW	0x0	disable_127_chk Disable 127 check
6	RW	0x0	skip_bksv_blacklist_chk Skip bksv blacklist check
5	RW	0x1	authenticated_en Authenticated or not authenticated 0: Authenticated 1: Not authenticated

Bit	Attr	Reset Value	Description
4	RW	0x0	av_encrypte_en AV content is encrypted enable 0: AV content is not encrypted 1: AV content is encrypted
3	RW	0x0	advanced_cipher_en advanced cipher enable 0: Advanced cipher is not enabled 1: Advanced cipher is enabled
2:0	RW	0x0	reserved

HDMI_reg58

Address: Operational Base + offset (0x0560)

Register58

Bit	Attr	Reset Value	Description
7:0	RW	0x00	rx_bcaps_value RX Bcaps value

HDMI_reg63

Address: Operational Base + offset (0x058c)

Register63

Bit	Attr	Reset Value	Description
7:0	RW	0x26	timer_100ms Registers for timer 100ms

HDMI_reg64

Address: Operational Base + offset (0x0590)

Register64

Bit	Attr	Reset Value	Description
7:0	RW	0x2c	timer_5s Registers for timer 5sec

HDMI_reg65

Address: Operational Base + offset (0x0594)

Register65

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3	RW	0x0	ddc_channel_no_ack DDC channels no acknowledge
2	RW	0x0	pj_mismatch Pj mismatch
1	RW	0x0	ri_mismatch Ri mismatch
0	RW	0x0	bksv_wrong Bksv is wrong

HDMI_reg6c

Address: Operational Base + offset (0x05b0)

Register6c

Bit	Attr	Reset Value	Description
7:0	RW	0x00	seed_an An seed for generate An

HDMI_reg7b

Address: Operational Base + offset (0x05ec)

Register7b

Bit	Attr	Reset Value	Description
7:0	RW	0x00	bksv part1 bksv

HDMI_reg7c

Address: Operational Base + offset (0x05f0)

Register7c

Bit	Attr	Reset Value	Description
7:0	RW	0x00	bksv part2 bksv

HDMI_reg7d

Address: Operational Base + offset (0x05f4)

Register7d

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	bksv part3 bksv

HDMI_reg7e

Address: Operational Base + offset (0x05f8)

Register7e

Bit	Attr	Reset Value	Description
7:0	RW	0x00	bksv part4 bksv

HDMI_reg7f

Address: Operational Base + offset (0x05fc)

Register7f

Bit	Attr	Reset Value	Description
7:0	RW	0x00	bksv part5 bksv

HDMI_reg80

Address: Operational Base + offset (0x0600)

Register80

Bit	Attr	Reset Value	Description
7:0	RW	0x00	tx_bcaps TX Bcaps

HDMI_reg81

Address: Operational Base + offset (0x0604)

Register81

Bit	Attr	Reset Value	Description
7:0	RW	0x00	bstate_part1 Bstate

HDMI_reg82

Address: Operational Base + offset (0x0608)

Register82

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	bstate_part2 Bstate

HDMI_reg95

Address: Operational Base + offset (0x0654)

Register95

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hdcp_fifo_first_wr_byte_addr HDCP KEY FIFO first write byte num address

HDMI_reg96

Address: Operational Base + offset (0x0658)

Register96

Bit	Attr	Reset Value	Description
7:0	RW	0x00	hdcp_fifo_first_rd_byte_addr HDCP KEY FIFO first read byte num address

HDMI_reg97

Address: Operational Base + offset (0x065c)

Register97

Bit	Attr	Reset Value	Description
7:2	RO	0x0	reserved
1	RW	0x0	hdcp_fifo_rd_addr8 HDCP KEY FIFO first read byte num address[8]
0	RW	0x0	hdcp_fifo_wr_addr8 HDCP KEY FIFO first write byte num address[8]

HDMI_reg98

Address: Operational Base + offset (0x0660)

Register98

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x03	hdcp_fifo_wr_rd_addr HDCP KEY FIFO write or read point address

HDMI_reg9c

Address: Operational Base + offset (0x0670)

Register9c

Bit	Attr	Reset Value	Description
7	RW	0x0	general_control_packet General control packet 1:enable 0:disable
6	RW	0x0	mpeg_source_frame_packet MPEG source InfoFrame packet 1:enable 0:disable
5	RW	0x0	source_descriptor_frame_packet Source product descriptor InfoFrame packet 1:enable 0:disable
4	RW	0x0	vendor_specific_frame_packet Vendor specific InfoFrame packet 1:enable 0:disable
3	RW	0x0	gamut_metadata_packet Gamut metadata packet 1:enable 0:disable

Bit	Attr	Reset Value	Description
2	RW	0x0	isrc1_packet ISRC1 packet 1:enable 0:disable
1	RW	0x0	acp_packet ACP packet 1:enable 0:disable
0	RW	0x0	generic_packet Generic packet 1:enable 0:disable

HDMI_reg9e

Address: Operational Base + offset (0x0678)

Register9e

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x1	auto_checksum_frame Auto checksum for InfoFrame 1:enable 0:disable It enables checksum calculation for any InfoFrame packets by hardware.

HDMI_reg9f

Address: Operational Base + offset (0x067c)

Register9f

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	packet_offset packet offset register for 0xa0~0xbe 8'h0: Generic packet 8'h1: ACP packet 8'h2: ISRC1 packet 8'h3: ISRC2 packet 8'h4: Gamut metadata packet 8'h5: Vendor specific InfoFrame 8'h6: AVI InfoFrame 8'h7: Source product descriptor InfoFrame packet 8'h8: Audio InfoFrame packet 8'h9: MPEG source InfoFrame

HDMI_rega0

Address: Operational Base + offset (0x0680)

Registera0

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega1

Address: Operational Base + offset (0x0684)

Registera1

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega2

Address: Operational Base + offset (0x0688)

Registera2

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega3

Address: Operational Base + offset (0x068c)

Registera3

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega4

Address: Operational Base + offset (0x0690)

Registera4

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega5

Address: Operational Base + offset (0x0694)

Registera5

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega6

Address: Operational Base + offset (0x0698)

Registera6

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega7

Address: Operational Base + offset (0x069c)

Registera7

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega8

Address: Operational Base + offset (0x06a0)

Registera8

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_rega9

Address: Operational Base + offset (0x06a4)

Registera9

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regaa

Address: Operational Base + offset (0x06a8)

Registeraa

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regab

Address: Operational Base + offset (0x06ac)

Registerab

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regac

Address: Operational Base + offset (0x06b0)

Registerac

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regad

Address: Operational Base + offset (0x06b4)

Registerad

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regae

Address: Operational Base + offset (0x06b8)

Registerae

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regaf

Address: Operational Base + offset (0x06bc)

Registeraf

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb0

Address: Operational Base + offset (0x06c0)

Registerb0

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb1

Address: Operational Base + offset (0x06c4)

Registerb1

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb2

Address: Operational Base + offset (0x06c8)

Registerb2

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb3

Address: Operational Base + offset (0x06cc)

Registerb3

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb4

Address: Operational Base + offset (0x06d0)

Registerb4

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb5

Address: Operational Base + offset (0x06d4)

Registerb5

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb6

Address: Operational Base + offset (0x06d8)

Registerb6

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb7

Address: Operational Base + offset (0x06dc)

Registerb7

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb8

Address: Operational Base + offset (0x06e0)

Registerb8

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regb9

Address: Operational Base + offset (0x06e4)

Registerb9

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regba

Address: Operational Base + offset (0x06e8)

Registerba

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbb

Address: Operational Base + offset (0x06ec)

Registerbb

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbc

Address: Operational Base + offset (0x06f0)

Registerbc

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbd

Address: Operational Base + offset (0x06f4)

Registerbd

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regbe

Address: Operational Base + offset (0x06f8)

Registerbe

Bit	Attr	Reset Value	Description
7:0	RW	0x00	After configure the packet offset register, these registers can configure any packet shown following. Use this function please refer to the HDMI specification at "Data Island Packet Definitions" Generic packet ACP packet ISRC1 packet ISRC2 packet Gamut metadata packet Vendor specific InfoFrame packet AVI InfoFrame packet Source product descriptor InfoFrame packet Audio InfoFrame packet MPEG source InfoFrame packet

HDMI_regc0

Address: Operational Base + offset (0x0700)

Registerc0

Bit	Attr	Reset Value	Description
7:1	RW	0x60	mask_int Mask for Interrupt 0: masked, 1: not mask [7] Interrupt for hot plug detect (HPD) [5] Interrupt for active Vsync edge [2] Interrupt for EDID Ready
0	RW	0x0	reserved

HDMI_regc1

Address: Operational Base + offset (0x0704)

Registerc1

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:1	RW	0x00	int_statu Interrupt status [7] Interrupt for hot plug detect (HPD) This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] Interrupt for active Vsync edge This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [2] Interrupt for EDID Ready This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.
0	RW	0x0	reserved

HDMI_regc2

Address: Operational Base + offset (0x0708)

Registerc2

Bit	Attr	Reset Value	Description
7:3	RW	0x0	int_mask Mask for interrupt: 0:masked, 1:not masked [7] for HDCP error [6] for bksv fifo ready [5] for bksv update [4] for authentication success [3] for ready to start authentication
2:0	RW	0x0	reserved

HDMI_regc3

Address: Operational Base + offset (0x070c)

Registerc3

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:3	RW	0x00	int_status Interrupt status [7] HDCP error Interrupt This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [6] bksv fifo ready This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] bksv update This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [4] authentication success This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [3] ready to start authentication This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.
2:0	RW	0x0	reserved

HDMI_regc4

Address: Operational Base + offset (0x0710)

Registerc4

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	int_mask Mask for interrupt: 0:masked,1:not masked [7] for HDCP soft mode ready [6] for HDCP authentication M0 ready [5] for first frame arrive [4] for HDCP An ready [3] [2] for HDCP encrypted [1] for HDCP not encrypted (av mute) [0] for HDCP not encrypted (no av mute)

HDMI_regc5

Address: Operational Base + offset (0x0714)

Registerc5

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0x00	int_status_group3 Interrupt status Group3 [7] HDCP soft mode ready This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [6] HDCP authentication M0 ready This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [5] 1st frame arrive This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [4] HDCP An ready This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [2] HDCP encrypted This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [1] HDCP not encrypted (av mute) This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit. [0] HDCP not encrypted (no av mute) This bit will active when the mask for this bit to be set 1. When Interrupt occurs, this bit will be equal to 1. Clear interrupt: write 1 to this bit.

HDMI_regc8

Address: Operational Base + offset (0x0720)

Registerc8

Bit	Attr	Reset Value	Description
7	RW	0x0	hot_plug_pin_status Hot plug pin status 1: Plug in, 0: Plug out
6	RW	0x0	reserved
5	RW	0x0	ddcsda_bus_status DDCSDA bus status
4	RW	0x0	ddcsel_bus_status DDCSCL bus status
3:0	RW	0x0	reserved

HDMI_regc9

Address: Operational Base + offset (0x0724)

Registerc9

Bit	Attr	Reset Value	Description
7:6	RW	0x1	video_bist_mode Video BIST mode 00: normal color bar. 01: special color bar. 10: black
5	RW	0x0	flush_en Flush enable. After enable it the screen will flush from color bar to black again and again. 1: enable 0: disable

Bit	Attr	Reset Value	Description
4	RW	0x1	disable_colorbar_bist_test Disable color bar BIST test 1: disable 0: enable
3:0	RW	0x0	reserved

HDMI_regce

Address: Operational Base + offset (0x0738)

Registerce

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x1	tmds_channel_sync The synchronization for TMDS channels The synchronization for TMDS channels is automatic after Reset the HDMI. But you can synchronization for TMDS channels manually. The operation for this function is: first send 0 to this bit, then send 1, and keep 1 into this bit.

HDMI_regd0

Address: Operational Base + offset (0x0740)

Registerd0

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6	RW	0x0	modify_start_bit_timing_hisense_tv Modify the start bit timing for Hisense TV 1: Modify the start bit timing for Hisense TV 0: Not modify
5	RW	0x0	reject_rec_cec_broadcast_message Reject receive CEC broadcast message 1: Reject receive CEC broadcast message 0: Not reject
4:3	RW	0x0	reserved

Bit	Attr	Reset Value	Description
2	RW	0x0	CEC_bus_free_time_cnt_en Enable count CEC bus free time 1: Enable count CEC bus free time 0: Not enable
1	RW	0x0	forbid_receive_cec_message Forbid receive CEC message 1: Forbid receive CEC message 0: Not forbid
0	RW	0x0	start_transmit_cec_message Start transmit CEC message 1: Start transmit CEC message 0: Not start

HDMI_regd1

Address: Operational Base + offset (0x0744)

Registerd1

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_rx_tx_data_in_fifo CEC RX/TX data in FIFO

HDMI_regd2

Address: Operational Base + offset (0x0748)

Registerd2

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	wr_cec_tx_data_addr Point address for write CEC TX data

HDMI_regd3

Address: Operational Base + offset (0x074c)

Registerd3

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x00	cec_rx_data_addr Point address for CEC RX data

HDMI_regd4

Address: Operational Base + offset (0x0750)

Registerd4

Bit	Attr	Reset Value	Description
7:0	RW	0x03	cec_clk_freq CEC working clock frequency register1

HDMI_regd5

Address: Operational Base + offset (0x0754)

Registerd5

Bit	Attr	Reset Value	Description
7:0	RW	0x09	cec_work_clk_freq CEC working clock frequency register1

HDMI_regd6

Address: Operational Base + offset (0x0758)

Registerd6

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x03	tx_block_length Length of TX blocks

HDMI_regd7

Address: Operational Base + offset (0x075c)

Registered7

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x00	rx_block_length Length of RX blocks

HDMI_regd8

Address: Operational Base + offset (0x0760)

Registerd8

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
7:0	RW	0xff	cec_tx_int_mask Mask for CEC TX Interrupts 0: masked 1: not mask [3] Interrupt for TX done [2] Interrupt for TX no ACK from follower [1] Interrupt for TX broadcast rejected [0] Interrupt for CEC line free time not satisfied

HDMI_regd9

Address: Operational Base + offset (0x0764)

Registerd9

Bit	Attr	Reset Value	Description
7:0	RW	0xff	cec_rx_int_mask Mask for CEC RX Interrupts 0: masked 1: not mask [4] Interrupt for RX receive logic address error [3] Interrupt for RX receive glitch error [2] Interrupt for RX ACK detect overtime [1] Interrupt for RX sending broadcast reject [0] Interrupt for RX done

HDMI_regda

Address: Operational Base + offset (0x0768)

Registerda

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_tx_int CEC TX Interrupts [3] Interrupt for TX done [2] Interrupt for TX no ACK from follower [1] Interrupt for TX broadcast rejected [0] Interrupt for CEC line free time not satisfied

HDMI_regdb

Address: Operational Base + offset (0x076c)

Registerdb

Bit	Attr	Reset Value	Description
7:0	RW	0x00	cec_tx_int CEC RX Interrupts [4] Interrupt for RX receive logic address error [3] Interrupt for RX receive glitch error [2] Interrupt for RX ACK detect overtime [1] Interrupt for RX sending broadcast reject [0] Interrupt for RX done

HDMI_regdc

Address: Operational Base + offset (0x0770)

Registerdc

Bit	Attr	Reset Value	Description
7:0	RW	0xd0	signal_free_time_l Signal free time length_L

HDMI_regdd

Address: Operational Base + offset (0x0774)

Registerdd

Bit	Attr	Reset Value	Description
7:0	RW	0x20	signal_free_time_h Signal free time length_H

HDMI_regde

Address: Operational Base + offset (0x0778)

Registerde

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved
3:0	RW	0x0	dev_addr Device logic address

HDMI_rege0

Address: Operational Base + offset (0x0780)

Registere0

Bit	Attr	Reset Value	Description
7:6	RW	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x1	tmads_clk_source_sel TMDS clock source 0:select TMDS clock from PLL 1:select TMDS clock generated by serializer
4	RW	0x0	tmads_clk_phase_sel TMDS clock phase selection 0: select default phase for TMDS clock; 1: select synchronized phase for TMDS clock with regard to TMDS data
3	RW	0x0	turn_on_reference_current turn on reference current 0: turn on the reference current; 1: cut off reference current for TMDS drivers
2	RW	0x0	hdmi_band_gap_pd HDMI Band gap power down. 1:Active
1	RW	0x1	hdmi_pll_pd HDMI PLL power down. 1:Active
0	RW	0x1	tmads_channel_pd TMDS channel power down. 1:Active

HDMI_rege1

Address: Operational Base + offset (0x0784)

Register1

Bit	Attr	Reset Value	Description
7:4	RW	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x1	clk_channel_driver_en Clock channel driver enable 0: disable 1: enable
2:0	RW	0x7	data_channels_driver_en Three data channels driver enable [2]-ch2 [1]-ch1 [0]-ch0 0: disable 1: enable

HDMI_rege2

Address: Operational Base + offset (0x0788)

Register2

Bit	Attr	Reset Value	Description
7:4	RW	0xa	clk_driver_strength Clock channel main-driver strength 0000~1111: the strength from low to high
3:0	RW	0xa	data_driver_strength Three data channels main-driver strength 0000~1111: the strength from low to high

HDMI_rege3

Address: Operational Base + offset (0x078c)

Register3

Bit	Attr	Reset Value	Description
7	RW	0x0	reserved
6:4	RW	0x0	pre_emphasis_strength Pre-emphasis strength 000~111: the strength from 0 to high

Bit	Attr	Reset Value	Description
3:2	RW	0x3	clk_driver_strength Clock channel pre-driver strength Slew rate from low to high 00~11: the strength from low to high
1:0	RW	0x3	data_driver_strength Three data channels pre-driver strength Slew rate from low to high 00~11: the strength from low to high

HDMI_rege7

Address: Operational Base + offset (0x079c)

Register7

Bit	Attr	Reset Value	Description
7:0	RW	0x1e	feedback_dividing_ratio_part1 The value of feedback dividing ratio

HDMI_rege8

Address: Operational Base + offset (0x07a0)

Register8

Bit	Attr	Reset Value	Description
7:1	RW	0x0	reserved
0	RW	0x0	feedback_dividing_ratio_part2 The value of feedback dividing ratio

HDMI_reged

Address: Operational Base + offset (0x07b4)

Registerd

Bit	Attr	Reset Value	Description
7:5	RW	0x0	reserved
4:0	RW	0x03	pre_dividing_ratio The value of pre-dividing ratio

Note1: There are some bits of registers have not description in the registers table above, are reserved for other using, please keep it into default value.

10.7 Application Notes

This chapter describes how to bring up HDMI transmitter in your system. As shown few examples below, these introduce the basically HDMI transmitter application, likes, the Hot Plug Detect, EDID read back, multiple audio format input and different video resolution displaying. You can easily configure these functions with proper registers value setting by configuration BUS. There is a few comfortable configuration BUS for customer choosing, likes, the I2C BUS, SPI BUS, or internal parallel BUS.

10.7.1 Initial Operation

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 48K sample I2S format audio input. It is easily for customer to turn on HDMI transmitter without doing more complex operation. Following the steps shown below you will easy bring up HDMI TX system.

Initial Steps:

- Step1:**Power supply to HDMI TX.
- Step2:**Reset system by pin_rst_n.
- Step3:** Wait Hot Plug.
- Step4:** Read EDID.
- Step5:**Active vclk through pin_vclk
- Step6:** Power on analog part.
Send 0x20 to register 0xe0. //Power on PLL and ANA TX core.
- Step7:**Configuration mode reg at addr 0x00 if needed.
- Step8:**Configuration Video format if needed.
- Step9:**Configuration Audio format if needed.
- Step10:** Configuration mode reg, power on digital part and select tmds_clk for configuration.
Send 0x71 to register 0x00.
- Step11:** Synchronize analog module.
Send 0x00 to register 0xce.
Send 0x01 to register 0xce.

10.7.2 Hot Plug Detect

Hot Plug Detect is a special feature for HDMI transmitter spying the state on the HDMI port.

You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations. The following is a step by step instruction for detecting the hot plug in and out.

Hot Plug in Steps:

- Step1:** Send 0x17 to register 0x00.
- Step2:** Plug HDMI receiver in.

Step3: Check the interrupt from signal pin_int.

If the pin_int shows high, that means the HDMI transmitter interrupt have generated.

Step4: Check the interrupt.

Read the bit7 of the register 0xc1. If bit7=1'b1 that means the hot plug interrupt valid, otherwise there is other interrupt. Then send the 1'b1 to bit7 of register 0xc1 to clean up the hot plug interrupt.

Step5: Check if really HDMI receiver plug in.

Read the bit7 of the register 0xc8. If bit7=1'b1 that means hot plug in was really happen, otherwise there is may be a glitch on the HPD port.

Hot Plug out Steps:

Step1: HDMI transmitter at working state.

Step2: Plug HDMI receiver out.

Step3: Check the interrupt from signal pin_int.

If the pin_int shows high, that means the HDMI transmitter interrupt have generated.

Step4: Check the interrupt.

Read the bit7 of the register 0xc1. If bit7=1'b1 that means the hot plug interrupt valid, otherwise there is other interrupt. Then send the 1'b1 to bit7 of register 0xc1 to clean up the hot plug interrupt.

Step5: Check if really HDMI receiver plug out.

Read the bit7 of the register 0xc8. If bit7=1'b0 that means hot plug out was really happen, otherwise there is may be a glitch on the HPD port.

10.7.3 Read EDID

Read EDID is a function that can make the HDMI transmitter to read the HDMI receiver's Extended Display Identification Data (EDID) in order to discover the HDMI receiver's configuration and capabilities. HDMI transmitter can choose the appropriate audio and video format for playing and displaying by the HDMI receiver through the use of the EDID. Besides, HDMI transmitter support the reading Enhanced Extended Display Identification Data (E-EDID) if HDMI receiver have this enhanced structure.

The following describes how to read E-EDID through HDMI transmitter. The total E-EDID is 512bytes data, which is divided into 2 segments. Each segment has 256bytes data. The Read E-EDID function is only read 128bytes data from HDMI receiver at each time. So, you must read 4 times that can read total 512bytes data back.

Prepare read E-EDID 512bytes Steps:

Step1: Send 0x17 to register 0x00.

System power down mode. Register clock use system clock.

Step2:HDMI transmitter detected Hot Plug in.

Step3:Define DDC clock (SCL) frequency $F_{scl} = 100K$.

$F_{scl} = F_{reg_clk} / (4 * X)$. $X = \{\text{register 0x4c, register 0x4b}\}$.

Note F_{reg_clk} is the frequency of the register clock, which can be

configured equal to TMDS clock or system clock by bit2 of the register 0x00.

Assume the system clock is 20MHz.

Send 0x32 to register 0x4b, Send 0x00 to register 0x4c.

Step4:Enable EDID Ready interrupt.

Send 0x84 to register 0xc0

Read E-EDID segment 0x00 256bytes Steps:

Step1:Set EDID FIFO initial address.

Send 0x00 to register 0x4f

Step2:Set EDID first word address, read first 128bytes.

Send 0x00 to register 0x4e

Step3:Set EDID segment address.

Send 0x00 to register 0x4d

Step4:Waiting and check EDID interrupt from pin_int.

Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. Then send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.

Step5:Read first 128bytes EDID data from EDID FIFO.

for (i = 0, i < 128, i = i + 1)

Read data from register 0x50.

Step6:Set EDID FIFO initial address again.

Send 0x00 to register 0x4f

Step7:Set EDID first word address, read last 128bytes.

Send 0x80 to register 0x4e

Step8:Set EDID segment address.

Send 0x00 to register 0x4d

Step9:Waiting and check EDID interrupt from pin_int.

Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. Then send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.

Step10:Read last 128bytes EDID data from EDID FIFO.

for (i = 0, i < 128, i = i + 1)

Read data from register 0x50.

Read E-EDID segment 0x01 256bytes Steps:

Step1:Set EDID FIFO initial address.

Send 0x00 to register 0x4f

Step2:Set EDID first word address, read first 128bytes.

Send 0x00 to register 0x4e

Step3:Set EDID segment address.

Send 0x01 to register 0x4d

Step4:Waiting and check EDID interrupt from pin_int.

Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. Then send the 1'b1 to bit2 of register 0xc1 to clean

up the EDID Ready interrupt.

Step5:Read first 128bytes EDID data from EDID FIFO.

for (i = 0, i < 128, i = i + 1)

Read data from register 0x50.

Step6:Set EDID FIFO initial address again.

Send 0x00 to register 0x4f

Step7:Set EDID first word address, read last 128bytes.

Send 0x80 to register 0x4e

Step8:Set EDID segment address.

Send 0x01 to register 0x4d

Step9:Waiting and check EDID interrupt from pin_int.

Check the EDID Ready state from bit2 of register 0xc1. If bit2 = 1'b1 that means EDID data ready. Then send the 1'b1 to bit2 of register 0xc1 to clean up the EDID Ready interrupt.

Step10:Read last 128bytes EDID data from EDID FIFO.

for (i = 0, i < 128, i = i + 1)

Read data from register 0x50.

Note: The segment address must be sent at each time when read 128bytes E-EDID data.

10.7.4 Audio Input Configuration

HDMI transmitter audio support either SPDIF or four channel I2S input. SPDIF input supports audio sampling rates from 32 to 192 KHz. The I2S input supports from 2-channel to 8-channel audio up to 192 KHz. The default audio format is I2S input with 8 channels. The audio sample rate is 48K.

The following describes how to configure audio input format into I2S input with 2 channels and the sample rate is 44.1K.

Audio input requirement:

SD0 input (2 Channels I2S input)

WS (fs) = 44.1 KHz

SCK = 64fs

MCLK = 256fs

Configure Audio Input Format Steps:

Step1:Select I2S input.

Send 0x01 to register 0x35

Step2: Select SD0 input.

Send 0x04 to register 0x38

Step3: Select N/CTS for sample rate = 44.1 KHz.

Send 0x18 to register 0x40

Send 0x80 to register 0x41

The following describes how to configure audio input format into I2S input with 8 channels and the sample rate is 44.1K.

Audio input requirement:

SD[3:0] input (8 Channels I2S input)
WS (fs) = 44.1 KHz
SCK = 64fs
MCLK = 256fs

Configure Audio Input Format Steps:

Step1: Select I2S input.

Send 0x01 to register 0x35

Step2: Select SD[3:0] input.

Send 0x3c to register 0x38

Send 0x00 to register 0x39

Step3: Select N/CTS for sample rate = 44.1 KHz.

Send 0x18 to register 0x40

Send 0x80 to register 0x41

10.7.5 Video Input Configuration

HDMI transmitter support RGB/YCbCr 24/30/36bit video input with different resolution. The default video format is RGB24bit input at resolution of 1080P@60.

The following describes how to configure video input format into RGB24bit input at resolution of 480P@60, 720P@60 or 1080P@60.

Video input requirement:

24bit RGB 4:4:4 Source.

Resolution is 480P@60, 720P@60 or 1080P@60.

Configure Video Input Format Steps:

Step1: Select configure for video format.

Send 0x06 to register 0x9f

Step2: Configure the AVI info to HDMI RX.

Send 0x82 to register 0xa0 //HB0

Send 0x02 to register 0xa1 //HB1

Send 0x0d to register 0xa2 //HB3

Send 0x00 to register 0xa3 //PB0: checksum is auto set, needn't set this register

Send 0x00 to register 0xa4 //PB1

Send 0x08 to register 0xa5 //PB2

Send 0x70 to register 0xa6 //PB3

Send 0x10 to register 0xa7 //PB4: VID 1920*1080P@60

Send 0x40 to register 0xa8 //PB5

Note: Select correct VID for displaying.

Send 0x02 for 720*480P@60.

Send 0x04 for 1280*720P@60.

Send 0x05 for 1920*1080I@60.

Send 0x10 for 1920*1080P@60.

Send 0x11 for 720*576P@50.
 Send 0x13 for 1280*720P@50.
 Send 0x14 for 1920*1080I@50.
 Send 0x1f for 1920*1080P@50.

The detail configuration for AVI information, please refer to the HDMI specification (8.2.1) and CEA-861-D (6.3).

10.7.6 Low Power Mode

HDMI Transmitter can be configured into Low Power Mode at special customer works mode. The following is a step by step instruction to describe how to configure our HDMI Transmitter into this mode.

Low Power Enter Steps:

Step1:HDMI Transmitter working.
Step2:Low Power analog module.
 Send 0x00 to register 0xe1. //Drive disable
 Send 0x2f to register 0xe0.
Step3:Assign pin_vclk = 1'b0 or 1'b1.

Low Power Quit Steps:

Step1:Reset system by pin_rst_n.
Step2: Wait Hot Plug.
Step3: Read EDID.
Step4:Active vclk through pin_vclk
Step5:Bring up analog module.
 Send 0x2d to register 0xe0. //PLL power on
 Send 0x2c to register 0xe0. //TX power on
 Send 0x28 to register 0xe0. //BG power on
 Send 0x20 to register 0xe0. //Bias enable
 Send 0x0f to register 0xe1. //driver enable
Step6:Configuration mode reg at addr 0x00 if needed.
Step7:Configuration Video format if needed.
Step8:Configuration Audio format if needed.
Step9: Configuration mode reg, power on digital part and select tmds_clk for configuration.
 Send 0x71 to register 0x00.
Step10: Synchronize analog module.
 Send 0x00 to register 0xce.
 Send 0x01 to register 0xce.

10.7.7 CEC Operation

The CEC line is used for high-level user control of HDMI-connected devices. You can control this function by using the interrupt signal and proper registers

from the HDMI transmitter with few operations.

The following is a step by step instruction for CEC TX operations and CEC RX operations.

CEC TX steps

(Send the Command:Standby (0x36) for example)

Step1: Set logic address for CEC(logic address = 1).

Send 0x01 to register 0xde.

Step2: Configure the divide numbers for internal reference clock.

Send 0x03 to register 0xd4 and 0x09 to register 0xd5. **See Note1 for details.**

Step3: Configure the value for signal free time counter.

Send 0xd0 to register 0xdc and 0x20 to register 0xdd. **See Note2 for details.**

Step4: Configure point addressfor write CEC TX data.

Send 0x00 to register 0xd2.

Step5: Configure TX data FIFO (the Command of Standby).

Send 0x10 to register 0xd1, then, send 0x36 to register 0xd1.

The data 0x01 is for the Header Block, in which the high 4bits is for the initiator, the low 4bits is for the destination.

The data 0x36 is for the Data Block, it indicate the command for standby.

Step6: Configure TX data length of this packet. The length is 2.

Send 0x02 to register 0xd6.

Step7:Enable count CEC bus free time.

Send 0x04 to register 0xd0.

Step8: Waiting 16.8ms for CEC bus free.

Step9: Begin TX.

Send 0x05 to register 0xd0.

Step10: Waiting and check interrupt of CEC TX done.

Waiting the interrupt, then, read the value of register 0xda, if the value is 0x01 that means CEC command was transmitted successfully. At last, send 0x01 to register 0xda to clear up this interrupt.

CEC RX steps:

Step1: Set logic address for CEC(logic address = 1).

Send 0x01 to register 0xde.

Step2: Configure the divide numbers for internal reference clock. **See Note1 for details.**

Send 0x03 to register 0xd4 and 0x09 to register 0xd5.

Step3: Configure the point addressfor CEC RX data.

Send 0x00 to register 0xd3.

Step4: Waiting CEC TX send CEC packet to our HDMI Transmitter, then check interrupt of CEC.

Read the value of register 0xdb, if the value is 0x80,that means CEC

command was received successfully. Then send 0x80 to register 0xdb to clear up this interrupt.

Step5: Read the RX packet length.

Read the value of the register 0xd7.

Step6: Read the received CEC packet.

Read the value of the register 0xd1 according to the RX packet length. If the length is 2, please read twice from the register 0xd1.

Note1: The system clock(Default value $F_{sys} = 20\text{MHz}$ from `pin_sys_clk`), register 0xd4 and 0xd5 are used to configure the CEC logic to generate a reference clock($F_{ref} = 0.5\text{ MHz}$, $T_{ref} = 2\mu\text{s}$), which is used to control the CEC signal's generation. The following is the formula for generating reference clock 0.5MHz.

$$F_{ref} = F_{sys} / ((\text{register } 0xd4 + 1) * (\text{register } 0xd5 + 1)).$$

Under the default 20MHz system clock, the values of register 0xd4 and 0xd5 are 0x03 and 0x09.

*Note2: Before attempting to transmit or re-transmit a frame, a device shall ensure that the CEC line has been inactive for a number of bit periods. For example, the signal free time is $7 * 2.4\text{ms} = 16.8\text{ms}$ (the bit time is 2.4ms). According to the $16.8\text{ms} / 2\mu\text{s} = \{\text{register } 0xdd, \text{register } 0xdc\}$, so the register 0xdd=0x20 and register 0xdc= 0xd0.*

10.7.8 HDCP Operation

HDCP is designed to protect the transmission of Audiovisual Content between an HDCP Transmitter and an HDCP Receiver. You can control this function by using the interrupt signal and proper registers from the HDMI transmitter with few operations.

The following is a step by step instruction for HDCP operation.

HDCP operation steps (skip BKS black list check) :

Example Condition: Video Format : 1920×1080p@59.94/60Hz

Step1: Select the TMDS clock to configure registers.

Send 0x01 to register 0x00.

Step2: Write HDCP transmitter's Akey to the chip. **See Note1 for details.**

for(i=0; i <= 39 ; i = i + 1)

begin

hdcp_wdata_temp = akey[i];

for (j=0 ; j < 7 ; j = j + 1)

begin

Send hdcp_wdata_temp[7:0] to register 0x98;

hdcp_wdata_temp = hdcp_wdata_temp >> 8;

end

end

Step3: Write HDCP transmitter's AKSV1 to the chip. **See Note1 for details.**

hdcp_wdata_temp = pre_ksv1

for (i = 0, i < 5, i = i + 1)

```
begin
  Send hdcp_wdata_temp[7:0] to register 0x98;
  hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step4: Write HDCP transmitter's AKSV2 to the chip. **See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv2
for (i = 0, i < 5, i = i + 1)
begin
  Send hdcp_wdata_temp[7:0] to register 0x98;
  hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step5: Check the key_ready signal.

Read the value of register 0x54, if the value is 0x01, that means the Akey and AKSV were load into the chip successfully.

Step6: Configure the DDC frequency. **See Note2 for details.**

Send 0x73 to register 0x4b.

Send 0x01 to register 0x4c.

Step7: Configure the HDCP function.

Send 0x77 to register 0x53.

Step8: Open the mask for HDCP interrupt.

Send 0xff to register 0xc2.

Send 0xff to register 0xc4.

Step9: Start the HDCP authentication.

Send 0x96 to register 0x52.

Step10: Checking HDCP interrupt.

Read the value of register 0xc3 and register 0xc5, if the value of register 0xc3 is 0x10 and the value of register 0xc5 is 0x65, that is means the HDCP authentication was successfully finished.

HDCP operation steps (**not skip BKS black list check**) :

Example Condition: Video Format : 1920×1080p@59.94/60Hz

Step1: Select the TMDS clock to configure registers.

Send 0x01 to register 0x00.

Step2: Write HDCP transmitter's Akey to the chip. **See Note1 for details.**

```
for(i=0; i <= 39 ; i = i+ 1 )
begin
  hdcp_wdata_temp = akey[i];
  for ( j=0 ; j < 7 ; j = j + 1 )
  begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
  end
end
```

Step3: Write HDCP transmitter's AKSV1 to the chip. **See Note1 for details.**

```
hdcp_wdata_temp = pre_ksv1
for (i = 0, i < 5, i = i + 1)
begin
  Send hdcp_wdata_temp[7:0] to register 0x98;
  hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step4: Write HDCP transmitter's AKSV2 to the chip. **See Note1 for**

details.

```
hdcp_wdata_temp = pre_ksv2
for (i = 0, i < 5, i = i + 1)
begin
    Send hdcp_wdata_temp[7:0] to register 0x98;
    hdcp_wdata_temp = hdcp_wdata_temp >>8;
end
```

Step5: Check the key_ready signal.

Read the value of register 0x54, if the value is 0x01, that means the Akey and AKSV were load into the chip successfully.

Step6: Configure the DDC frequency. **See Note2 for details.**

Send 0x73 to register 0x4b.

Send 0x01 to register 0x4c.

Step7: Configure the HDCP function.

Send 0x37 to register 0x53(do not skip the BKSv blacklist check).

Step8: Open the mask for HDCP interrupt.

Send 0xff to register 0xc2.

Send 0xff to register 0xc4.

Step9: Start the HDCP authentication.

Send 0x96 to register 0x52.

Step10: Check the BKSv.

Wait for INT from register c3 bit5(bksv_update), then read register 66~register 6a for BKSv values to check whether the BKSv is in the revocation list. If the BKSv is not in the revocation list, write 1 to register 52 bit6(bksv_pass), and authentication will continue. Else if the BKSv is in the revocation list, write 1 to register 52 bit5(bksv_fail), and authentication will stop.

Step11: Checking HDCP interrupt.

Read the value of register 0xc3 and register 0xc5, if the value of register 0xc3 is 0x10 and the value of register 0xc5 is 0x65, that is means the HDCP authentication was successfully finished.

Note1: For HDCP's akey and KSV write, use the TEST KEYS in HDCP specification for example

```
akey[0] = 56'h4da4588f131e69;
akey[1] = 56'h1f823558e65009;
akey[2] = 56'h8a6a47abb9980d;
akey[3] = 56'hf3181b52cbc5ca;
akey[4] = 56'hfb147f6896d8b4;
akey[5] = 56'he08bc978488f81;
akey[6] = 56'ha0d064c8112c41;
akey[7] = 56'hb39d5a28242044;
akey[8] = 56'hb928b2bdad566b;
akey[9] = 56'h91a47b4a6ce4f6;
akey[10] = 56'h5600f8205e9d58;
akey[11] = 56'h8c7fb706ee3fa0;
akey[12] = 56'hc02d8c9d7cbc28;
akey[13] = 56'h561261e54b9f05;
akey[14] = 56'h74f0de8ccac1cb;
akey[15] = 56'h3bb8f60efcdb6a;
akey[16] = 56'ha02bbb16b22fd7;
akey[17] = 56'h482f8e46785498;
akey[18] = 56'h66ae2562274738;
akey[19] = 56'h3d4952a323ddf2;
akey[20] = 56'he2d231767b3a54;
```

```
akey[21] = 56'h4d581aede66125;
akey[22] = 56'h326082bf7b22f7;
akey[23] = 56'hf61b463530ce6b;
akey[24] = 56'h360409f0d7976b;
akey[25] = 56'ha1e105618d49f9;
akey[26] = 56'hc98e9dd1053406;
akey[27] = 56'h20c36794426190;
akey[28] = 56'h964451ceac4fc3;
akey[29] = 56'h3e904504e18c8a;
akey[30] = 56'h290010579c2dfc;
akey[31] = 56'hd7943b69e5b180;
akey[32] = 56'h54c7ea5bdd7b43;
akey[33] = 56'h74fb5887c790ba;
akey[34] = 56'h935cfa364e1de0;
akey[35] = 56'h03075e159a11ae;
akey[36] = 56'h05d3408a78fb01;
akey[37] = 56'h0059a5d7a04db3;
akey[38] = 56'h373b634a2c9e40;
akey[39] = 56'h2573bbb4562041;
```

```
pre_ksv1 = 40'hb70361f714;
pre_ksv2 = 40'hb70361f714;
```

Note2: For DDC frequency configuration

In the HDCP specification, the frequency value of DDC(F_{ddc}) support only up to 100Kbps, and now we select the TMDS clock as the reference clock of DDC, and under the condition of 1920×1080p@59.94/60Hz, the frequency of TMDS(F_{TMDS}) is 148.5MHz. Pay attention, internally we use the 4 times of DDC frequency to generate the SCL. So

$X = F_{TMDS}/F_{ddc}/4 = 'h173$, So the values of register 0x4b and 0x4c are 0x73 and 0x01.

10.7.9 NORMAL Operation Example at 1080P

After the description of HDMI Transmitter configuration above, the following example shows an entire configuration for HDMI Transmitter works on the 1080P mode.

Audio input requirement:

SD0 input (2 Channels I2S input)
 WS (fs) = 48 KHz
 SCK = 64fs
 MCLK = 256fs

Video input requirement:

24bit RGB 4:4:4 Source.
 Resolution is 1080P@60.

Setup Steps:

- Step1:**Power on HDMI TX.
- Step2:** Configure the input signals.
 Assign pin_test_en = 1'b0.
- Step3:**Reset HDMI Transmitter.
 Assign 0 to the signal pin_rst_n and then assign 1.
- Step4:**System power down.
 Send 0x17 to register 0x00.

Step5:Detect Hot Plug In.

Step6:Read EDID.

Step7: Configure video input format.

Step8:Configure audio input format.

Step9:Assign video and audio source to HDMI Transmitter.

Step10:System power on.

Send 0x01 to register 0x00.

Step11: Now, HDMI Transmitter is ready to go. Start your operation.

10.8 Color Bar Test

We provide a methodology to verify the function of HDMI transmitter test chip immediately after packaged. The following is a step by step instruction for bringing up HDMI transmitter working at built-in color bar mode.

The default HDMI transmitter is configured to 24bit RGB 1080P resolution video with 8 channel 48K sample I2S format audio input.

Setup Steps:

Step1:Power on HDMI Transmitter test chip.

Step2: Configure the input signals.

Assign pin_test_en = 1'b0.

Give the system clock through pin_sys_clk. Assume pin_sys_clk equal to 20MHz.

Give the pixel clock through pin_vclk. The frequency of the pixel clock must be set according your test requirement. For example, the 720P color bar use 74.25MHz, the 1080P color bar use 148.5MHz.

A set of video input signals except pin_vclk can correspond to low level.

A set of audio input signals can be also correspond to low level. If you want test audio fast, you can input 8 channels (pin_sd[3:1] can be set to low level, if you only use 2 channels) 48K I2S audio, that is the default configuration.

Step3:Reset HDMI Transmitter test chip.

Assign 0 to the signal pin_rst_n and then assign 1.

Step4: Power on analog part.

Send 0x20 to register 0xe0. //Power on PLL and ANA TX core.

Step5:System power down.

Send 0x67 to register 0x00.

Step6:Plug in HDMI cable with HDMI TV connected.

Step7:Select built-in color bar mode.

Send 0x00 to register 0xc9

Step8:Select configure for video format.

Send 0x06 to register 0x9f

Step9:Select proper color bar for displaying.

When pin_vclk = 27MHz, send 0x02 to register 0xa7, for 480P@60 color bar.

When pin_vclk = 74.25MHz, send 0x04 to register 0xa7, for 720P@60 color bar.

When pin_vclk = 148.5MHz, send 0x10 to register 0xa7, for 1080P@60 color bar.

Step10: System power on.

Send 0x71 to register 0x00.

After done the steps shown above, you can check the color bar display on TV.

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Chapter 11 APS

11.1 Overview

The APS (audio protocol switch) controller which can arbitrary switch audio protocol is a bridge between Audio Codec and external application controller.

- arbitrary audio protocol switch, including I2S normal, left-justified, right-justified, PCM early ,late1, late2 and late3
- Support 16 ~ 32 bits audio data transfer
- Support master and slave mode
- Support 2 channels audio transmitting and receiving in I2S and PCM mode
- Support up to 192kHz sample rate
- Support I2S normal, left and right justified mode serial audio data transfer
- Support PCM early, late1, late2, late3 mode serial audio data transfer
- Support MSB or LSB first serial audio data transfer
- Support 16 to 31 bit audio data left or right justified in 32-bit wide FIFO
- Support two 16-bit audio data store together in one 32-bit wide location

11.2 Block Diagram

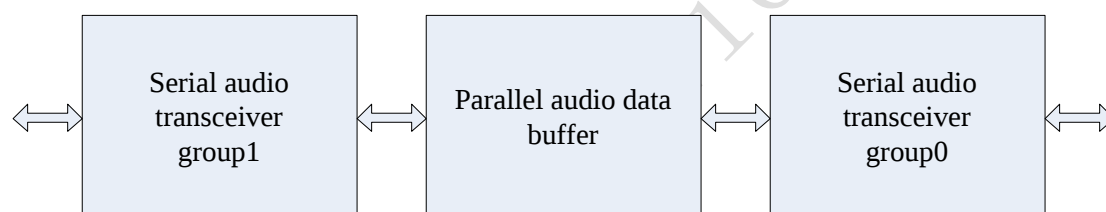


Fig. 11-1 APS Block Diagram

11.3 Function description

The common usage of APS block in this chip is switch PCM protocol in group1 to I2S protocol in group0. The groups1 interface is tightly connected with I2S1_PAD which is external Bluetooth interface. And group0 interface is an internal interface which is connected with Audio Codec. The supported audio protocol in this block is the following.

11.3.1 I2S normal mode

This is the waveform of I2S normal mode. For LRCK (lrck_rx/ lrck_tx) signal, it goes low to indicate left channel and high to right channel. For SD (sdo, sdi) signal, it transfers MSB or LSB first and sends the first bit one SCLK clock cycle after LRCK changes. The range of SD signal width is from 16 to 32bits.

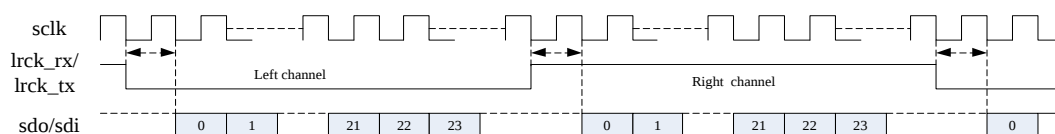


Fig. 11-2 I2S normal mode timing format

11.3.2 I2S left justified mode

This is the waveform of I2S left justified mode. For LRCK (lrck_rx / lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sdo, sdi) signal, it transfers MSB or LSB first and sends the first bit at the same time when LRCK changes. The range of SD signal width is from 16 to 32bits.

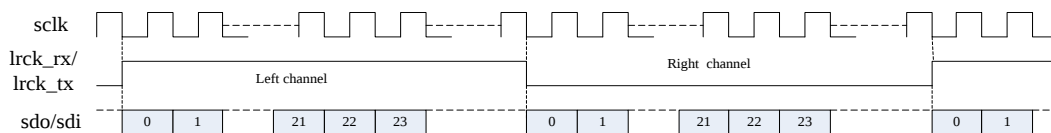


Fig. 11-3 I2S left justified mode timing format

11.3.3 I2S right justified mode

This is the waveform of I2S right justified mode. For LRCK (lrck_rx/ lrck_tx) signal, it goes high to indicate left channel and low to right channel. For SD (sdo, sdi) signal, it transfers MSB or LSB first; but different from I2S normal or left justified mode, its data is aligned to last bit at the edge of the LRCK signal. The range of SD signal width is from 16 to 32bits.

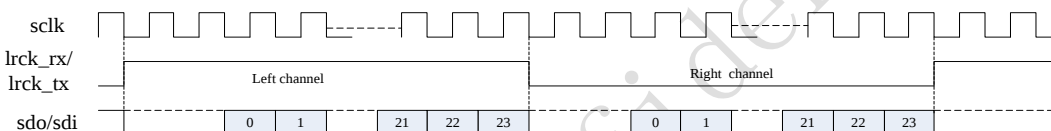


Fig. 11-4 I2S right justified mode timing format

11.3.4 PCM early mode

This is the waveform of PCM early mode. For LRCK (lrck_rx/ lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sdo, sdi) signal, it transfers MSB or LSB first and sends the first bit at the same time when LRCK goes high. The range of SD signal width is from 16 to 32bits.

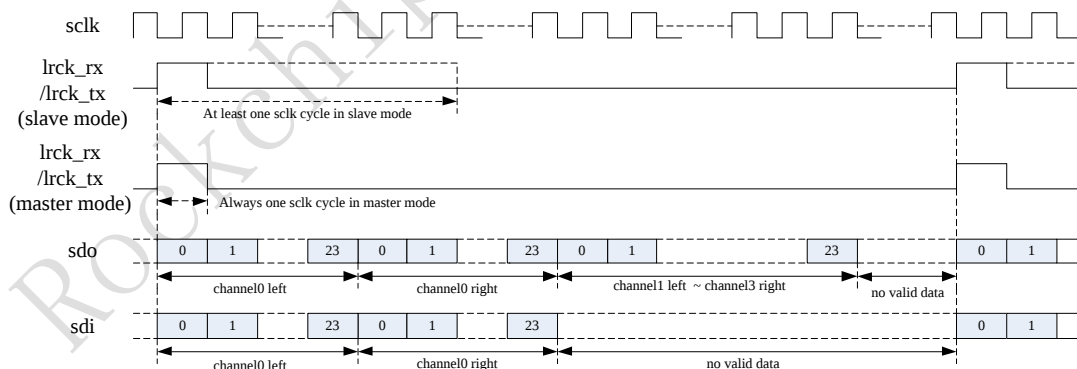


Fig. 11-5 PCM early mode timing format

11.3.5 PCM late1 mode

This is the waveform of PCM early mode. For LRCK (lrck_rx/ lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sdo, sdi) signal, it transfers MSB or LSB first and sends the first bit one SCLK clock cycle after LRCK goes high. The range of SD signal width is from 16 to 32bits.

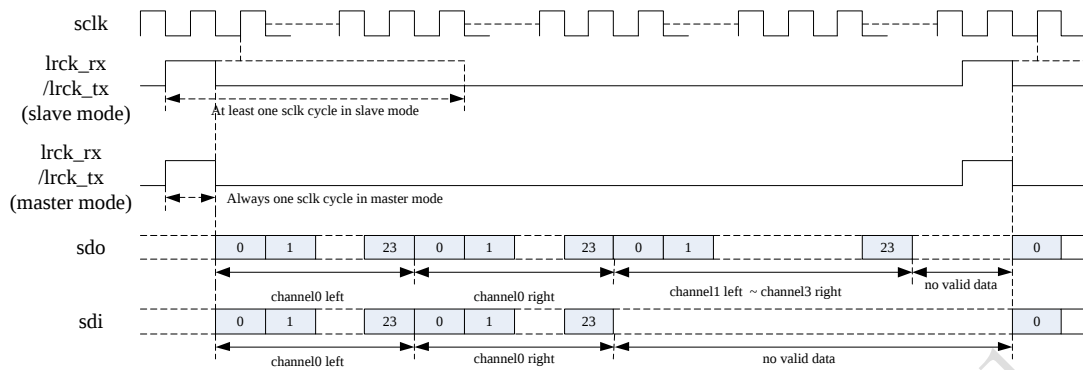


Fig. 11-6 PCM late1 mode timing format

11.3.6 PCM late2 mode

This is the waveform of PCM early mode. For LRCK (lrck_rx/ lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sdo, sdi) signal, it transfers MSB or LSB first and sends the first bit two SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

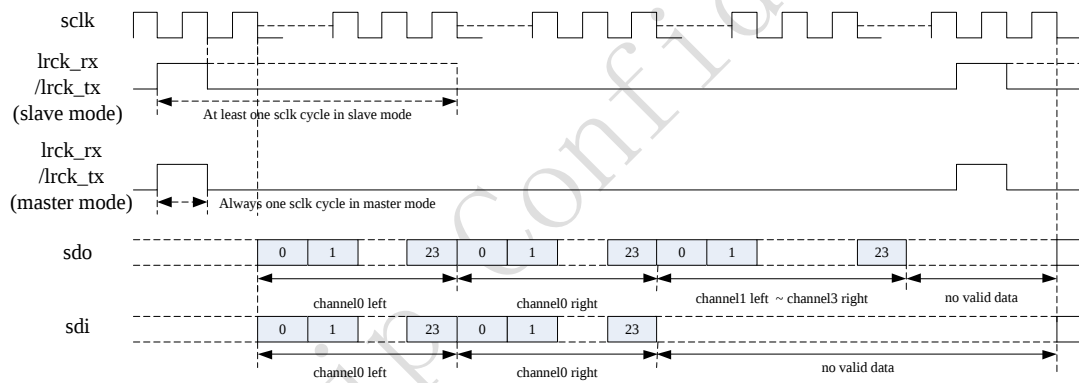


Fig. 11-7 PCM late2 mode timing format

11.3.7 PCM late3 mode

This is the waveform of PCM early mode. For LRCK (lrck_rx/ lrck_tx) signal, it goes high to indicate the start of a group of audio channels. For SD (sdo, sdi) signal, it transfers MSB or LSB first and sends the first bit three SCLK clock cycles after LRCK goes high. The range of SD signal width is from 16 to 32bits.

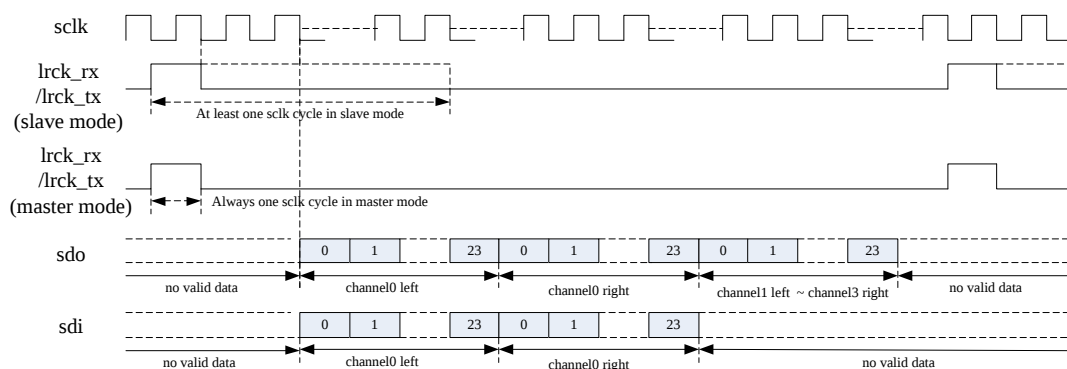


Fig. 11-8 PCM late3 mode timing format

11.4 Register description

Details refer to Chapter I2C

Chapter 12 Audio Codec

12.1 Overview

The ADC with 16 to 24bit resolution, DAC with 16 to 18bit resolution and power amplifier are integrated in the Audio Codec.

Key Features

- Pure logic process, no need for Mixed signal process.
- Very low power, can be made <6.5mA in 3.3V for playback.
- 18 to 24 bit high order Sigma-Delta modulation for DAC with >93 dB SNR.
- 16 to 18 bit high order Sigma-Delta modulation for ADC with >90 dB SNR.
- Digital interpolation and decimation filter integrated.
- Line-in, microphone and speaker out interface.
- On-chip analog post filter and digital filters.
- Single-ended or differential microphone input.
- Automatic gain control for smooth audio recording.
- Sampling rate of 8k/12k/16k/24k/32k/48k/44.1k/96k Hz
- Support 16ohm to 32ohm headphone and speaker phone output.
- 3.3V analog +/-10% power supply for analog and 1.2/1.1/1.0V for digital core.
- Mono, Stereo supported.

12.2 Block Diagram

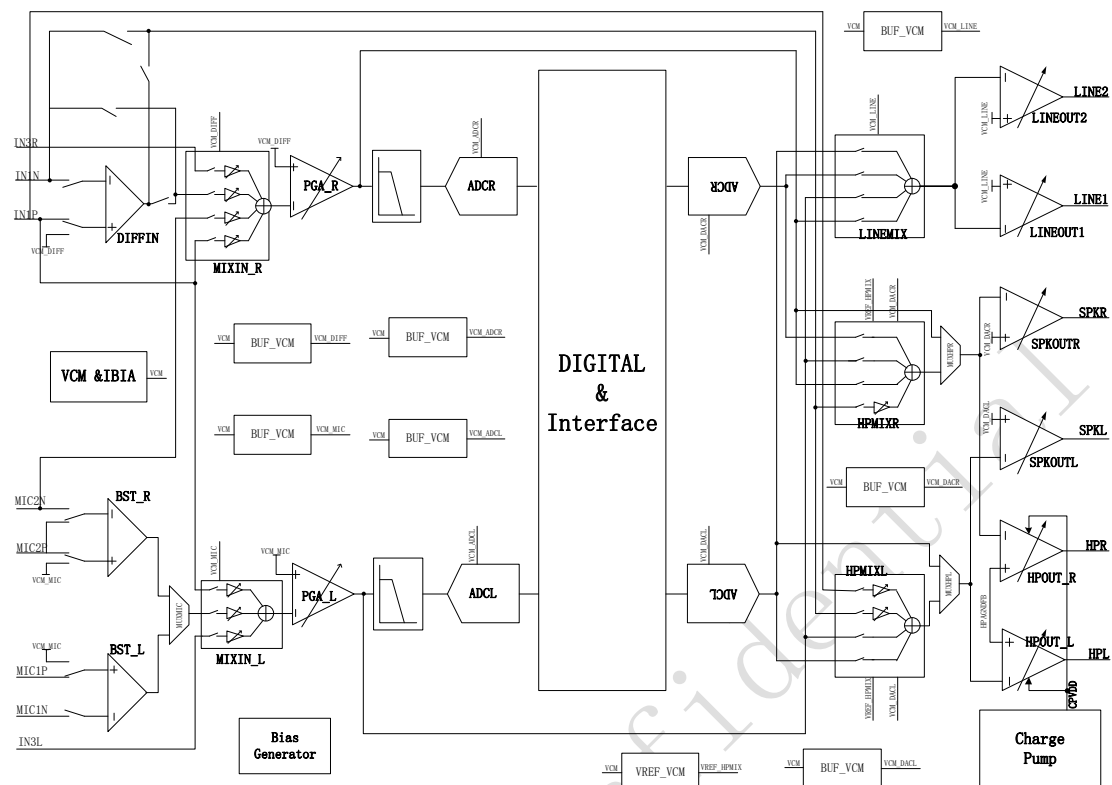


Fig. 12-1 Audio Codec Block Diagram

12.3 Electrical Specification

TEST Conditions

AVDD=3.3V, T_A=27°C, 1 KHz sine input, fs=6.144MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs						
Full-scale Input Signal Level	V _{INFS}	GAIN _B =0dB GAIN _P =0dB		1.1		V _{rms}
Input resistance	R _{MICIN}	GAIN _B =0dB		14.5		KΩ
		GAIN _B =20dB		79.75		KΩ
Input Gain Boost						
Programmable GAIN	GAIN _B		0		20	dB
Programmable GAIN Step Size			-	20	-	dB
Gain of PGA_L(PGA_R)						
Boost Gain	GAIN _P		-18		28.5	dB
Boost Gain Step Size				1.5		dB
Analogue to Digital Converter (ADC)						
Signal to Noise Ratio	SNR	GAIN _P =0dB GAIN _B =0dB		90		dB

Channel Separation				70		dB
Digital to Analogue Converter(DAC) ,without load						
DAC output GAIN	GAIN _D		-39		6	dB
DAC output GAIN Step Size				1.5		dB
Signal to Noise Ratio	SNR	GAIN _D =0dB		93		dB
Total Harmonic Distortion	THD	GAIN _D =0dB Without Load		-80		dB
Total Harmonic Distortion	THD	GAIN _D =0dB With 32Ω load		-70		dB

12.4 Function description

12.4.1 Digital Interface

The Codec has the I2S PCM interface of audio data stream in for DAC and out for ADC, both of which can be configured in master or slave mode. Different audio data formats are available for different operating modes, which are demonstrated in below table.

Table 12-1 Supported Data Formats in Different Modes

Data Formats	ADC		DAC	
	Master	Slave	Master	Slave
Left Justified	✓	×	✓	✓
Right Justified	✓	✓	✓	✓
I ² S	✓	✓	✓	✓
DSP/PCM mode A	✓	✓	✓	✓
DSP/PCM mode B	✓	×	✓	✓

I2S PCM interface supports five audio data formats: Left Justified mode, Right Justified mode, I²S mode, DSP/PCM mode A and mode B. They are valid when the device operates as a master or slave.

For Left Justified mode, the data format is illustrated in Fig. 12-2. The MSB is valid at the first rising edge of sck after ws transition is done. The other valid bits up to the LSB are transmitted sequentially. Due to varied word length, different sck frequency and sample rate, some unused sck cycles may appear before every ws transition, which means the data in this period is invalid.

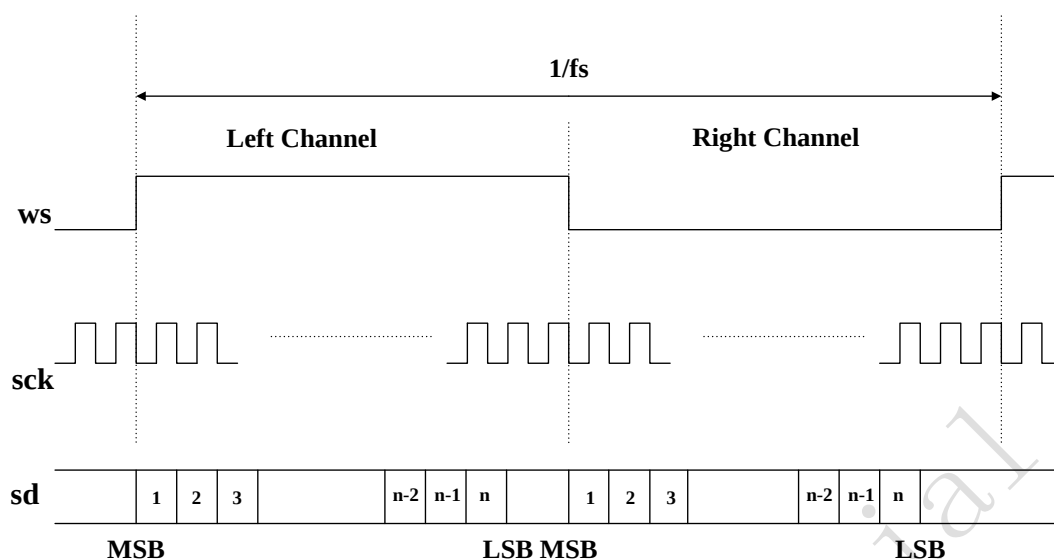


Fig. 12-2 Left Justified Mode (assuming n-bit word length)

For Right Justified mode, the data format is shown in Fig. 12-3. The LSB becomes valid at the last rising edge of **sck** before **ws** transition is done. As the MSB is transmitted first, the other valid bits up to the MSB are followed in order. Due to varied word length, different **sck** frequency and sample rate, some unused **sck** cycles may exist after every **ws** transition, which means the data in this period is invalid.

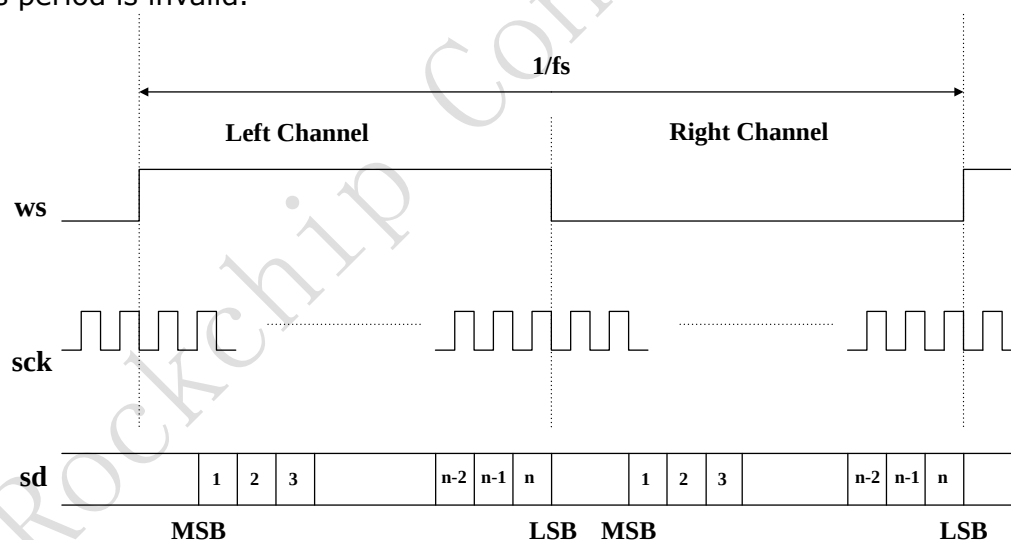


Fig. 12-3 Right Justified Mode (assuming n-bit word length)

For I²S mode, the data format is depicted in Fig. 12-4. The MSB becomes available at the second rising edge of **sck** when **ws** transition is done. The other valid bits up to the LSB are transmitted in order. Due to varied word length, different **sck** frequency and sample rate, some unused **sck** cycles may appear between the LSB of the current sample and the MSB of the next one, which means the data in this period can be ignored.

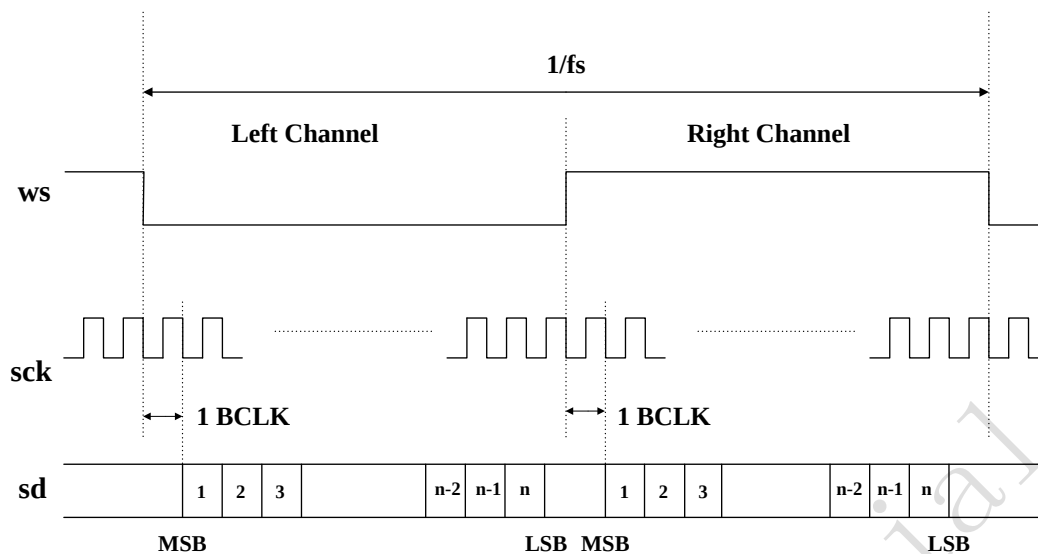


Fig. 12-4 I2S Mode (assuming n-bit word length)

For DSP/PCM mode, the left channel data is transmitted first, followed by right channel data. For DSP/PCM mode A/B, the MSB is available at the second and first rising edge of sck after the rising edge of ws respectively, as shown in Fig. 12-5 and Fig. 12-6. Based on word length, sck frequency and sample rate, there may be some invalid data between the LSB of the right channel data and the next sample.

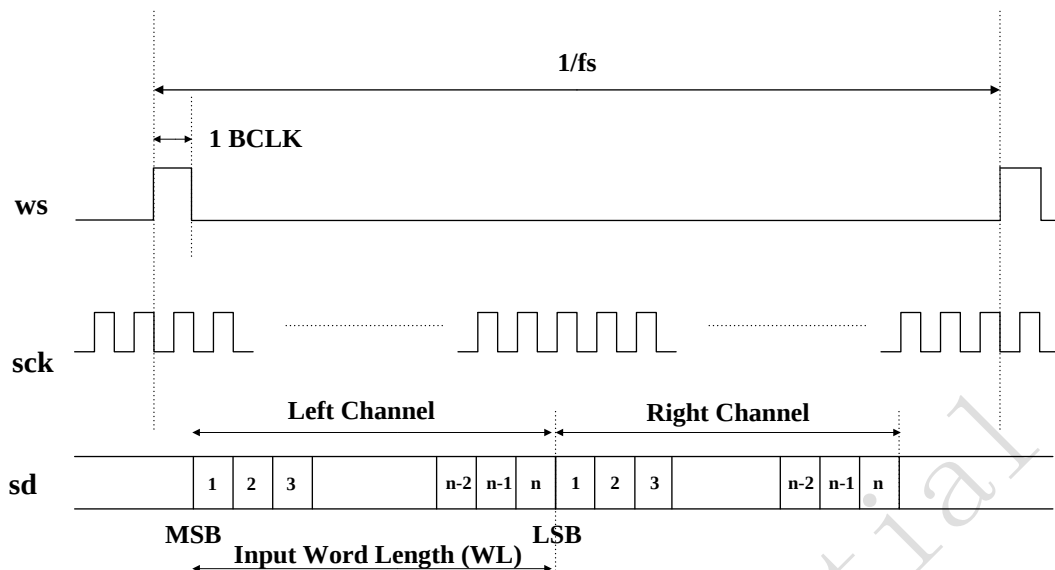


Fig. 12-5 DSP/PCM Mode A (assuming n-bit word length)

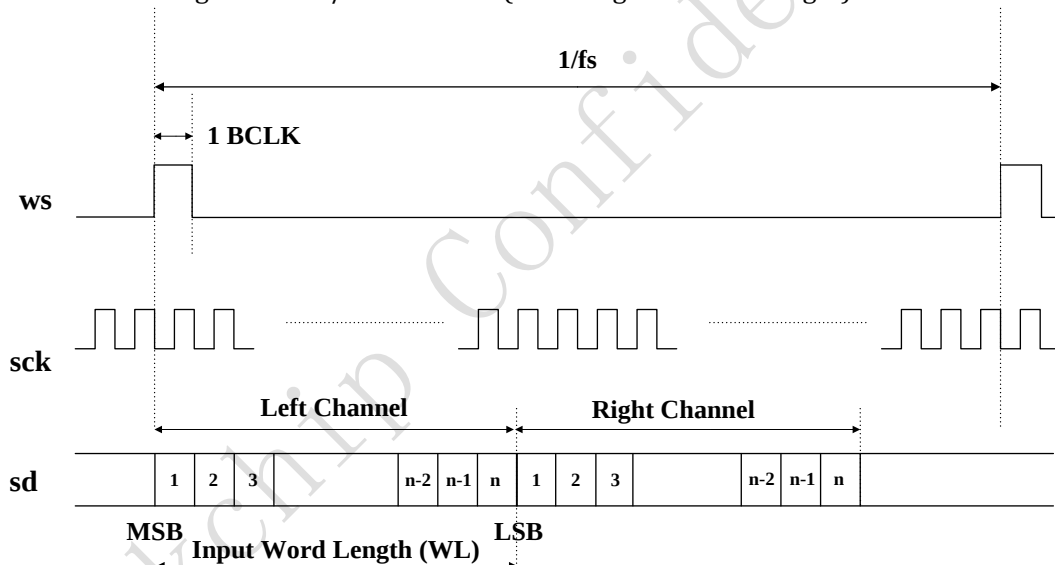


Fig. 12-6 DSP/PCM Mode B (assuming n-bit word length)

12.4.2 Analog Interface

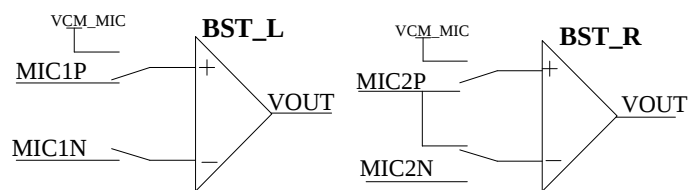


Fig. 12-7 MicroPhone Input

There are two microphone input channels, left and right channel. In each channel, there are two differential inputs, and they can be configured as either single-ended input or differential inputs by the microphone PGA (BST_L and BST_R).

In left channel, microphone inputs are MICIN and MICIP. When working in

single-ended configuration, the input signal should be input through MIC2N.

In right channel, microphone inputs are MIC2N and MIC2P. When working in single-ended configuration, the input signal can be fed through either MIC2N or MIC2P.

Microphone PGA has two gains to amplify the input signal, that is, 0dB and +20dB.

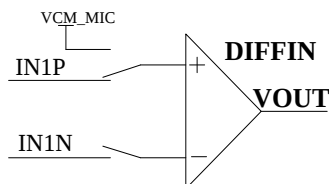


Fig. 12-8 Line-In Input

There are 4 line inputs, including IN1P, IN1N, IN3L, and IN3R. They can be mixed into the input and output paths for different purposes. All line inputs can work as single-ended input, and IN1P and IN1N can work as differential inputs. When differential signals are inputted through IN1P and IN1N, they can be converted into single-ended signal by DIFFIN PGA. DIFFIN PGA can also be configured as single-ended input mode or differential input mode.

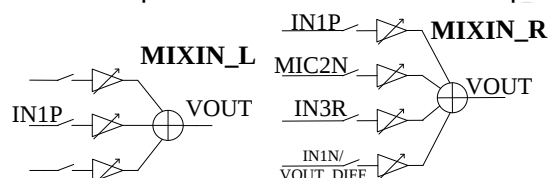


Fig. 12-9 Input Mixer

Microphone input and Line input signals can be mixed together by input mixer. There are two input channel mixers, MIXIN_L and MIXIN_R. In left input channel, the output of microphone PGA, line input IN3L and IN1P can be mixed by the left input mixer. In right input channel, line input IN3R, IN1P, IN1N, output of DIFFIN PGA, and microphone input MIC2N can be mixed by the right input mixer.

All mixer inputs have independent gain control within the range from -12dB to +6dB. The increment is 3dB.

Automatic Level Control (ALC) function is to adjust the signal level, which is sent into ADC. ALC will measure the signal magnitude and compare it to the defined threshold. Then it will adjust the ALC controlled PAG (PGA_L and PGA_R) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

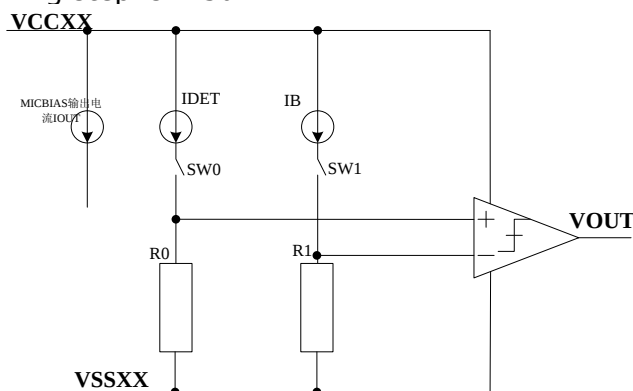


Fig. 12-10 Microphone Bias

Two microphone bias outputs are available to bias external microphones, MICBIAS1 and MICBIAS2. The bias voltage can vary from $0.5 \times AVDD$ to $0.85 \times AVDD$ with a step of $0.05 \times AVDD$.

The output current of each microphone bias is monitored by a current detection circuit. It will compare the output current to a reference current and output the comparison result to digital circuit. The reference current can be selected from 0.1mA to 1.5mA with 0.2mA step.

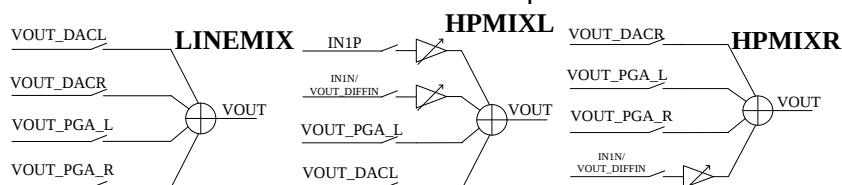


Fig. 12-11 Output Mixer

DAC output, line input and bypass of ADC input can be mixed by output mixer. There are three output channel mixers, including HPMIXL, HPMIXR and LINEMIX.

In HPMIXL mixer, output of left channel DAC, bypass of left channel ADC input, IN1P, IN1N or output of DIFFIN PGA can be mixed.

In HPMIXR mixer, output of right channel DAC, bypass of left channel ADC input, bypass of right channel ADC input, IN1P, IN1N or output of DIFFIN PGA can be mixed.

In LINEMIX mixer, output of left channel DAC, output of right channel DAC, bypass of left channel ADC input and bypass of right channel ADC input can be combined together.

Mixer inputs of IN1P, IN1N or output of DIFFIN PGA have an attenuation control from -21dB to 0dB with a step of 3dB.

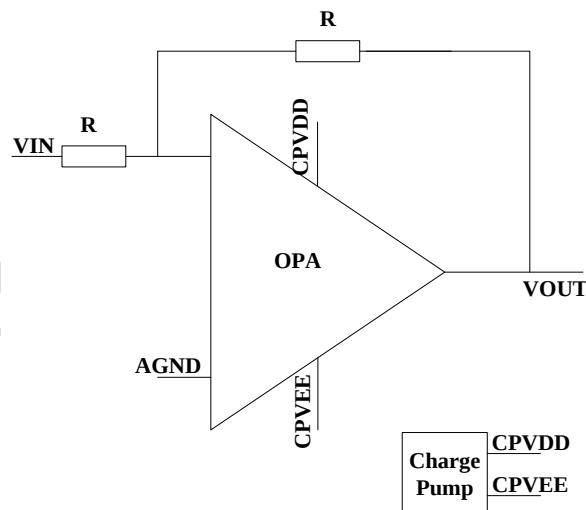


Fig. 12-12 HeadPhone output

The left and right channel headphone outputs (HPL and HPR) can drive 16 or 32Ω headphone. A charge pump circuit is employed to provide negative supply for headphone driver. Then the DC voltage of headphone output signal can be brought down to ground, instead of $AVDD/2$, which can eliminate the requirement of external DC-blocking capacitor.

The headphone driver can choose mixer output or DAC output as input. It has a gain range from -39dB to +6dB with a step of 1.5dB.

The left and right channel speaker outputs (SPKOUTL and SPKOUTR) can directly drive 16 or 32Ω speaker, or drive 8Ω speaker through additional power

amplifier.

The speaker driver can also choose mixer output or DAC output as input, and has a gain range from -39dB to +6dB with a step of 1.5dB.

The line outputs, LINE1 and LINE2, can work as differential outputs or two single-ended outputs. Output of LINEMIX is input to the line output driver with a gain range from -39dB to +6dB. The tuning step is 1.5dB.

12.4.3 Interface Relationship

Fig. 12-13 and Fig. 12-14 illustrate the relationship between I2S interface and the parallel audio data in ADC and DAC channels.

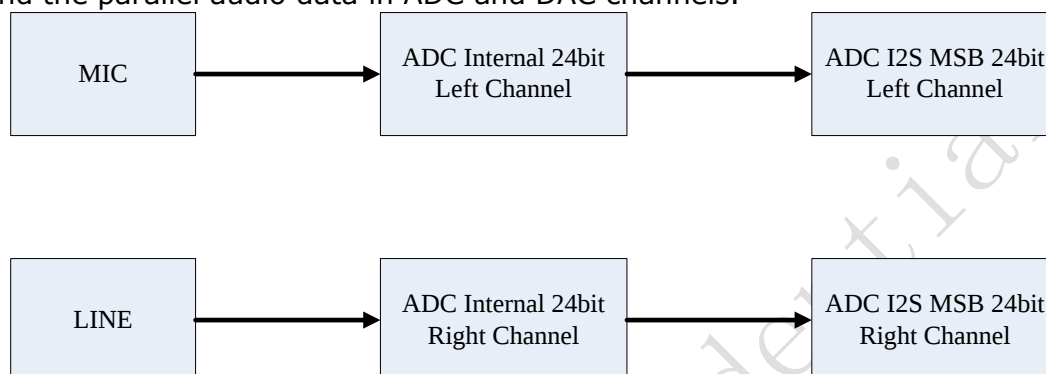


Fig. 12-13 ADC Channels Relationship

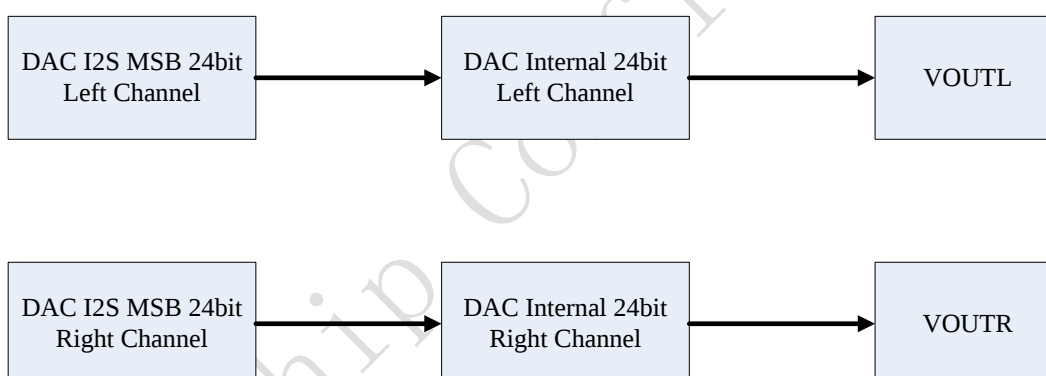


Fig. 12-14 DAC Channels Relationship

12.5 Register description

12.5.1 Register Summary

Name	Offset	Size	Reset Value	Description
Codec_REG0	0x0000	W	0x00000003	Codec register 0
Codec_REG2	0x0008	W	0x00000050	Codec register 2
Codec_REG3	0x000c	W	0x0000000e	Codec register 3
Codec_REG4	0x0010	W	0x00000050	Codec register 4
Codec_REG5	0x0014	W	0x0000000e	Codec register 5
Codec_REG15	0x003c	W	0x0000007c	Codec register 15
Codec_REG16	0x0040	W	0x00000099	Codec register 16

Name	Offset	Size	Reset Value	Description
Codec_REG17	0x0044	W	0x00000024	Codec register 17
Codec_REG18	0x0048	W	0x0000001f	Codec register 18
Codec_REG19	0x004c	W	0x00000024	Codec register 19
Codec_REG20	0x0050	W	0x00000004	Codec register 20
Codec_REG21	0x0054	W	0x0000003f	Codec register 21
Codec_REG22	0x0058	W	0x00000024	Codec register 22
Codec_REG23	0x005c	W	0x00000024	Codec register 23
Codec_REG24	0x0060	W	0x000000cc	Codec register 24
Codec_REG25	0x0064	W	0x000000cc	Codec register 25
Codec_REG26	0x0068	W	0x000000ff	Codec register 26
Codec_REG27	0x006c	W	0x0000003f	Codec register 27
Codec_REG28	0x0070	W	0x0000001f	Codec register 28
Codec_REG29	0x0074	W	0x0000003c	Codec register 29
Codec_REG30	0x0078	W	0x000000ff	Codec register 30
Codec_REG31	0x007c	W	0x00000000	Codec register 31
Codec_REG32	0x0080	W	0x00000000	Codec register 32
Codec_REG33	0x0084	W	0x00000060	Codec register 33
Codec_REG34	0x0088	W	0x00000060	Codec register 34
Codec_REG35	0x008c	W	0x000000e0	Codec register 35
Codec_REG36	0x0090	W	0x000000e0	Codec register 36
Codec_REG37	0x0094	W	0x000000e0	Codec register 37
Codec_REG38	0x0098	W	0x000000e0	Codec register 38
Codec_REG39	0x009c	W	0x000000ff	Codec register 39
Codec_REG40	0x00a0	W	0x00000028	Codec register 40
Codec_REG41	0x00a4	W	0x0000000f	Codec register 41
Codec_REG42	0x00a8	W	0x00000036	Codec register 42
Codec_REG48	0x00c0	W	0x00000010	Codec register 48
Codec_REG49	0x00c4	W	0x00000025	Codec register 49
Codec_REG50	0x00c8	W	0x00000041	Codec register 50
Codec_REG51	0x00cc	W	0x0000002c	Codec register 51
Codec_REG52	0x00d0	W	0x00000000	Codec register 52
Codec_REG53	0x00d4	W	0x00000026	Codec register 53
Codec_REG54	0x00d8	W	0x00000040	Codec register 54
Codec_REG55	0x00dc	W	0x00000036	Codec register 55
Codec_REG56	0x00e0	W	0x00000020	Codec register 56
Codec_REG57	0x00e4	W	0x00000038	Codec register 57
Codec_REG64	0x0100	W	0x00000010	Codec register 64
Codec_REG65	0x0104	W	0x00000025	Codec register 65
Codec_REG66	0x0108	W	0x00000041	Codec register 66
Codec_REG67	0x010c	W	0x0000002c	Codec register 67

Name	Offset	Size	Reset Value	Description
Codec_REG68	0x0110	W	0x00000000	Codec register 68
Codec_REG69	0x0114	W	0x00000026	Codec register 69
Codec_REG70	0x0118	W	0x00000040	Codec register 70
Codec_REG71	0x011c	W	0x00000036	Codec register 71
Codec_REG72	0x0120	W	0x00000020	Codec register 72
Codec_REG73	0x0124	W	0x00000038	Codec register 73

Notes: **Size**: **B**- Byte (8 bits) access, **HW**- Half WORD (16 bits) access, **W**-WORD (32 bits) access

12.5.2 Detail Register Description

Codec_REG0

Address: Operational Base + offset (0x0000)

Codec register 0

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	Power reset bypass 1: bypass 0: not
5:2	RO	0x0	reserved
1	RW	0x1	Codec digital core reset This reset only reset the codec data path. 0: reset 1: work
0	RW	0x1	Codec system reset This signal will reset the registers which control all the digital and analog part. 0: reset 1: work

Codec_REG2

Address: Operational Base + offset (0x0008)

Codec register 2

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	ADC LRC Polarity 1: enable 0: disable
6:5	RW	0x2	ADC Valid Word Length in one 1/2Frame 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits

Bit	Attr	Reset Value	Description
4:3	RW	0x2	ADC mode 11: PCM Mode 10: I2S Mode 01: Left Justified Mode 00: Right Justified Mode Note. Same word length in 1/2frame and valid data is not supported in Right Justified Mode. For example, 32/24 or 24/20 is supported, but 32/32 or 24/24 is not supported. (1/2frame length/valid data length)
2	RO	0x0	reserved
1	RW	0x0	ADC Left-Right SWAP 1: enable 0: disable
0	RW	0x0	ADC type 1: Mono 0: Stereo

Codec_REG3

Address: Operational Base + offset (0x000c)

Codec register 3

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x0	ADC and DAC I2S Mode Select 1: master mode 0: slave mode
3:2	RW	0x3	ADC 1/2Frame Word Length 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
1	RW	0x1	ADC Reset 1: work 0: reset
0	RW	0x0	ADC Bit Clock Polarity 1: enable 0: disable

Codec_REG4

Address: Operational Base + offset (0x0010)

Codec register 4

Bit	Attr	Reset Value	Description
-----	------	-------------	-------------

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	DAC LRC Polarity 1: enable 0: disable
6:5	RW	0x2	DAC Valid Word Length in one 1/2Frame 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
4:3	RW	0x2	DAC mode 11: PCM Mode 10: I2S Mode 01: Left Justified Mode 00: Right Justified Mode Note. Same word length in 1/2frame and valid data is not supported in Right Justified Mode. For example, 32/24 or 24/20 is supported, but 32/32 or 24/24 is not supported. (1/2frame length/valid data length)
2	RW	0x0	DAC Left-Right SWAP 1: enable 0: disable
1:0	RO	0x0	reserved

Codec_REG5

Address: Operational Base + offset (0x0014)

Codec register 5

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3:2	RW	0x3	DAC 1/2Frame Word Length 11: 32 bits 10: 24 bits 01: 20 bits 00: 16 bits
1	RW	0x1	DAC reset 1: work 0: reset
0	RW	0x0	DAC Bit Clock polarity 1: enable 0: disable

Codec_REG15

Address: Operational Base + offset (0x003c)

Codec register 15

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x1	Power down signal of current source for ADC 1: Power down 0: Not
5	RW	0x1	Power down signal of reference Voltage buffer for MIC1、MIC2、MIXIN_L、PGA_L module 1: Power down 0: Not
4	RW	0x1	Power down signal of reference Voltage buffer for DIFFIN、MIXINR、PGA_R module 1: Power down 0: Not
3	RW	0x1	Power down signal of reference Voltage buffer for ADCL module 1: Power down 0: Work
2	RW	0x1	Power down signal of reference Voltage buffer for ADCR module 1: Power down 0: Work
1:0	RO	0x0	reserved

Codec_REG16

Address: Operational Base + offset (0x0040)

Codec register 16

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of BST_L module 1: Power down 0: Not
6	RW	0x0	The input mode selecting of BST_L 1: Single-ended input 0: Full differential input
5	RW	0x0	The gain control of BST_L 1: 20dB 0: 0dB
4	RW	0x1	Mute signal of BST_L 1: MUTE 0: Normal work

Bit	Attr	Reset Value	Description
3	RW	0x1	Power down signal of BST_R module 1: Power down 0: Not
2	RW	0x0	The input mode selecting of BST_R 1: Single-ended input 0: Full differential input
1	RW	0x0	The gain control of BST_R 1: 20dB 0: 0dB
0	RW	0x1	Mute signal of BST_R 1: MUTE 0: Normal work

Codec_REG17

Address: Operational Base + offset (0x0044)

Codec register 17

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Power down signal of DIFFIN module 1: Power down 0: Not
4	RW	0x0	Input mode selecting of DIFFIN 1: Single-ended input 0: Full differential input
3	RW	0x0	The gain control of DIFFIN 1: 20dB 0: 0dB
2	RW	0x1	Mute signal of DIFFIN 1: MUTE 0: Work
1	RW	0x0	Select input signal to MIXIN_R from DIFFIN 1: Select 1N1N 0: Select output data of DIFFIN
0	RW	0x0	Select input signal to HPMIXL/HPMIXR from DIFFIN 1: Select 1N1N 0: Select output data of DIFFIN

Codec_REG18

Address: Operational Base + offset (0x0048)

Codec register 18

Bit	Attr	Reset Value	Description
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Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	The input of single-ended input mode of BST_R 1: Select MIC2P 0: Select MIC2N
5	RW	0x0	Select signal of MUXMIC module 1: Select BST_R output 0: Select BST_L output
4	RW	0x1	Power down signal of MIXIN_L 1: Power down 0: Work
3	RW	0x1	Mute signal of MIXIN_L 1: MUTE 0: Work
2	RW	0x1	select IN3L input to MIXIN_L 1: No selecting 0: Selecting
1	RW	0x1	Select IN1P input to MIXIN_L 1: No selecting 0: Selecting
0	RW	0x1	Select output of MUXMIC input to MIXIN_L 1: No selecting 0: Selecting

Codec_REG19

Address: Operational Base + offset (0x004c)

Codec register 19

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:3	RW	0x4	The gain control of MIXIN_L (input from MUXMIC) 000: -12dB 100: 0dB 111: 6dB Step: 3dB
2:0	RW	0x4	The gain control of MIXIN_L (input from IN1P) 000: -12dB 100: 0dB 111: 6dB Step: 3dB

Codec_REG20

Address: Operational Base + offset (0x0050)

Codec register 20

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x4	The gain control of MIXIN_L (input from IN3L) 000: -12dB 100: 0dB 111: 6dB Step: 3dB

Codec_REG21

Address: Operational Base + offset (0x0054)

Codec register 21

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Power down signal of MIXIN_R module 1: Power down 0: Work
4	RW	0x1	MUTE signal of MIXIN_R module 1: MUTE 0: Work
3	RW	0x1	select MIC2N input to MIXIN_R 1: No select 0: Select
2	RW	0x1	select IN1P input to MIXIN_R 1: No select 0: Select
1	RW	0x1	select IN3R input to MIXIN_R 1: No select 0: Select
0	RW	0x1	select output of DIFFIN or IN1N input to MIXIN_R 1: No select 0: Select

Codec_REG22

Address: Operational Base + offset (0x0058)

Codec register 22

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5:3	RW	0x4	The gain control of MIXIN_R (input from vout of DIFFIN or IN1N) 000: -12dB 100: 0dB 111: 6dB Step: 3dB
2:0	RW	0x4	The gain control of MIXIN_R (input from 1N3R) 000: -12dB 100: 0dB 111: 6dB Step: 3dB

Codec_REG23

Address: Operational Base + offset (0x005c)

Codec register 23

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:3	RW	0x4	The gain control of MIXIN_R (input from IN1P) 000: -12dB 100: 0dB 111: 6dB Step: 3dB
2:0	RW	0x4	The gain control of MIXIN_R (input from MIC2N) 000: -12dB 100: 0dB 111: 6dB Step: 3dB

Codec_REG24

Address: Operational Base + offset (0x0060)

Codec register 24

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of PGA_L module 1: Power down 0: Work
6	RW	0x1	The MUTE signal of PGA_L module 1: MUTE 0: Work
5	RO	0x0	reserved

Bit	Attr	Reset Value	Description
4:0	RW	0x0c	The gain control of PGA_L module 00000:-18dB 01100:0dB 11111:28.5dB Step:1.5dB

Codec_REG25

Address: Operational Base + offset (0x0064)

Codec register 25

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of PGA_R module 1: MUTE 0: Work
6	RW	0x1	The MUTE signal of PGA_R module 1: MUTE 0: Work
5	RO	0x0	reserved
4:0	RW	0x0c	The gain control of PGA_R module 00000:-18dB 01100:0dB 11111:28.5dB Step:1.5dB

Codec_REG26

Address: Operational Base + offset (0x0068)

Codec register 26

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of the bias current for HPOUTL and HPOUTR 1: power down 0: work
6	RW	0x1	Power down signal of current source for DAC module 1: Power down 0: Work
5	RW	0x1	Power down signal of high and low reference Voltage buffer for DACL 1: Power down 0: Work

Bit	Attr	Reset Value	Description
4	RW	0x1	Power down signal of reference Voltage buffer for DACL and SPKOUTL 1: Power down 0: Work
3	RW	0x1	Power down signal of high and low reference Voltage buffer for DACR 1: Power down 0: Work
2	RW	0x1	Power down signal of reference Voltage buffer for DACR and SPKOUTR(*) 1: Power down 0: Work
1	RW	0x1	Power down signal of reference Voltage buffer for LINEMIX、LINEOUT1 and LINEOUT2 1: Power down 0: Work
0	RW	0x1	Power down signal of reference Voltage buffer for HPMIXL and HPMIXR 1: Power down 0: Work

Codec_REG27

Address: Operational Base + offset (0x006c)

Codec register 27

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Initial signal of DACL module 0: Initialization 1: After the initialization
4	RW	0x1	Initial signal of DACR module 0: Initialization 1: After the initialization
3	RW	0x1	Power down signal of DACL module 1: Power down 0: Work
2	RW	0x1	Power down signal of DACR module 1: Power down 0: Work
1	RW	0x1	Power down signal of CLOCK module for DACR 1: Set to 1 0: Work

Bit	Attr	Reset Value	Description
0	RW	0x1	Power down signal of CLOCK module for DACL 1: Set to 1 0: Work

Codec_REG28

Address: Operational Base + offset (0x0070)

Codec register 28

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x1	Power down signal of LINEMIX module 1: Power down 0: Work
3	RW	0x1	select output of Analog Filiter_R to LINEMIX, LINER bypass path 1: don't select 0: select
2	RW	0x1	select output of Analog Filiter_L to LINEMIX, LINEL bypass path 1: don't select 0: select
1	RW	0x1	select output of DACR to LINEMIX 1: don't select 0: select
0	RW	0x1	select output of DACL to LINEMIX 1: don't select 0: select

Codec_REG29

Address: Operational Base + offset (0x0074)

Codec register 29

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Power down signal of HPMIXL module 1: Power down 0: Work
4	RW	0x1	Initial signal of HPMIXL module 1: Initialization 0: After the initialization
3	RW	0x1	Power down signal of HPMIXR module 1: Power down 0: Work

Bit	Attr	Reset Value	Description
2	RW	0x1	Initial signal of HPMIXR module 1: Initialization 0: After the initialization
1	RW	0x0	Selecting input of MUXHPL 1: Select DACL output signal 0: - Note: Before setting 1 , should power down HPMIXL
0	RW	0x0	Selecting input of MUXHPR 1: Select DACR output signal 0: - Note: Before setting 1 , should power down HPMIXR

Codec_REG30

Address: Operational Base + offset (0x0078)

Codec register 30

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	select output of DIFFIN or IN1N input to HPMIXL (Analog bypass path) 1: No select 0: Select
6	RW	0x1	select IN1P input to HPMIXL (Analog bypass path) 1: No select 0: Select
5	RW	0x1	select output of Analog_Filter_L input to HPMIXL (LINEL bypass path) 1: No select 0: select
4	RW	0x1	select output of DACL input to HPMIXL 1: No select 0: select
3	RW	0x1	select output of DIFFIN or IN1N input to HPMIXR (Analog bypass path) 1: No select 0: Select
2	RW	0x1	select output of Analog_Filter_R input to HPMIXR (LINER bypass path) 1: No select 0: Select

Bit	Attr	Reset Value	Description
1	RW	0x1	select output of Analog_Filter_L input to HPMIXR (LINEL bypass path) 1: No select 0: Select
0	RW	0x1	select output of DACR input to HPMIXR 1: No select 0: Select

Codec_REG31

Address: Operational Base + offset (0x007c)

Codec register 31

Bit	Attr	Reset Value	Description
31:3	RO	0x0	reserved
2:0	RW	0x0	The gain control of HPMIXL module (input from IN1P) 000: -21dB 111: 0dB Step: 3dB

Codec_REG32

Address: Operational Base + offset (0x0080)

Codec register 32

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5:3	RW	0x0	The gain control of HPMIXL module (input from output of DIFFIN or IN1N) 000: -21dB 111: 0dB Step: 3dB
2:0	RW	0x0	The gain control of HPMIXR module (input from output of DIFFIN or IN1N) 000: -21dB 111: 0dB Step: 3dB

Codec_REG33

Address: Operational Base + offset (0x0084)

Codec register 33

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved

Bit	Attr	Reset Value	Description
6	RW	0x1	Power down signal of LINEOUT1 module 1: Power down 0: Work
5	RW	0x1	MUTE signal of LINEOUT1 module 1: MUTE 0: Work
4:0	RW	0x00	LINEOUT1 gain control signal 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB

Codec_REG34

Address: Operational Base + offset (0x0088)

Codec register 34

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x1	Power down signal of LINEOUT2 module 1: Power down 0: Work
5	RW	0x1	MUTE signal of LINEOUT2 module 1: MUTE 0: Work
4:0	RW	0x00	LINEOUT2 gain control signal 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB

Codec_REG35

Address: Operational Base + offset (0x008c)

Codec register 35

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of SPKOUTL module 1: Power down 0: Work
6	RW	0x1	MUTE signal of SPKOUTL module 1: MUTE 0: Work

Bit	Attr	Reset Value	Description
5	RW	0x1	Initial signal of SPKOUTL module 1: Initialization 0: After the initialization
4:0	RW	0x00	SPKOUTL gain control signal 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB

Codec_REG36

Address: Operational Base + offset (0x0090)

Codec register 36

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of SPKOUTR module 1: Power down 0: Work
6	RW	0x1	Initial signal of SPKOUTR module 1: Initialization 0: After the initialization
5	RW	0x1	MUTE signal of SPKOUTR module 1: MUTE 0: Work
4:0	RW	0x00	SPKOUTR gain control signal 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB

Codec_REG37

Address: Operational Base + offset (0x0094)

Codec register 37

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of HPOUTL module 1: Power down 0: Work
6	RW	0x1	Initial signal of HPOUTL module 1: Initialization 0: After the initialization

Bit	Attr	Reset Value	Description
5	RW	0x1	MUTE signal of HPOUTL module 1: MUTE 0: Work
4:0	RW	0x00	HPOUTL gain control signal 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB

Codec_REG38

Address: Operational Base + offset (0x0098)

Codec register 38

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of HPOUTR module 1: Power down 0: Work
6	RW	0x1	Initial signal of HPOUTR module 1: Initialization 0: After the initialization
5	RW	0x1	MUTE signal of HPOUTR module 1: MUTE 0: Work
4:0	RW	0x00	HPOUTR gain control signal 00000: -39dB 11010: 0dB 11111: 6dB Step: 1.5dB

Codec_REG39

Address: Operational Base + offset (0x009c)

Codec register 39

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x1	Power down signal of MIC bias voltage 1 (MICBIAS1) buffer 1: Power down 0: Work
6	RW	0x1	Power down signal of MIC bias voltage 2 (MICBIAS2) buffer 1: Power down 0: Work

Bit	Attr	Reset Value	Description
5:3	RW	0x7	The level range control signal of MIC bias voltage 1(MICBIAS1) 000:1.0*VREF 111:1.7*VREF Step:0.1*VREF
2:0	RW	0x7	The level range control signal of MIC bias voltage 2(MICBIAS2) 000:1.0*VREF 111:1.7*VREF Step:0.1*VREF

Codec_REG40

Address: Operational Base + offset (0x00a0)

Codec register 40

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	MIC1(MICBIAS1 corresponding) key detection enable 1: Detection 0: Stop working
6	RW	0x0	MIC2(MICBIAS2 corresponding) key detection enable 1: Detection 0: Stop working
5:3	RW	0x5	MIC1(MICBIAS1 corresponding) key detection range setting signal 000:100uA 111:1500uA Step:200uA
2:0	RW	0x0	MIC2(MICBIAS2 corresponding) key detection range setting signal 000:100uA 111:1500uA Step:200uA

Codec_REG41

Address: Operational Base + offset (0x00a4)

Codec register 41

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved

Bit	Attr	Reset Value	Description
3	RW	0x1	The power down signal of the ADCL input zero-crossing detection: 1: Power down ,output 0 electrical level 0: Work
2	RW	0x1	The power down signal of the ADCR input zero-crossing detection: 1: Power down ,output 0 electrical level 0: Work
1	RW	0x1	The power down signal of the DACL input zero-crossing detection: 1: Power down ,output 0 electrical level 0: Work
0	RW	0x1	The power down signal of the DACR input zero-crossing detection: 1: Power down ,output 0 electrical level 0: Work

Codec_REG42

Address: Operational Base + offset (0x00a8)

Codec register 42

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Power down signal of CLOCK for ADCL module 1: Set to 1 0: Work
4	RW	0x1	Power down signal of Amplifier in ADCL module 1: Power down all operational amplifier 0: Normal work
3	RW	0x0	The reset signal of different levels integrator in ADCL module 1: Clear 0: Work
2	RW	0x1	Power down signal of CLOCK for ADCR module 1: Set to 1 0: Work
1	RW	0x1	Power down signal of Amplifier in ADCR module 1: Power down all operational amplifier 0: Normal work

Bit	Attr	Reset Value	Description
0	RW	0x0	The reset signal of different levels integrator in ADCR module 1: Clear 0: Work

Codec_REG48

Address: Operational Base + offset (0x00c0)

Codec register 48

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x1	There are two methods to generate the control signals(left channel) 0: Normal way 1: Jack way
3:0	RW	0x0	AGC hold time before gain is increased in normal mode.(left channel) 0000: 0ms 0001: 2ms 0010: 4ms 0011: 8ms 0100: 16ms 0101: 32ms 0110: 64ms 0111:128ms 1000:256ms 1001:512ms 1010: 1 s 1011~1111:0ms

Codec_REG49

Address: Operational Base + offset (0x00c4)

Codec register 49

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:4	RW	0x2	Decay (gain ramp-up) time(left channel) Normal MODE(reg_agc_mde =0) 0000:500us 0001:1ms 0010:2ms 0011:4ms 0100:8ms 0101:16ms 0110:32ms 0111:64ms 1000:128ms 1001:256ms 1010:512ms 1001~1111:512ms
3:0	RW	0x5	Attack (gain ramp-down) Time(left channel) Normal MODE(reg_agc_mde =0) 0000:125us 0001:250us 0010:500us 0011:1ms 0100:2ms 0101:4ms 0110:8ms 0111:16ms 1000:32ms 1001:64ms 1010:128ms 1011~1111:125us Normal MODE(reg_agc_mde =1) 0000:32us 0001:64us 0010:125us 0011:250us 0100:500us 0101:1ms 0110:2ms 0111:4ms 1000:8ms 1001:16ms 1010:32ms 1011~1111:32us

Codec_REG50

Address: Operational Base + offset (0x00c8)

Codec register 50

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	Determines the AGC mode of operation(left channel) 0:AGC mode(normal mode) 1:Limiter mode
6	RW	0x1	AGC users zero cross enable(left channel) 0:Disabled 1:Enabled, the AGC gain will update at zero cross enable
5	RW	0x0	When in the limiter mode, the low amplitude signal will recovery in two modes(left channel): 0:The gain will recovery to the value of the reg_pga_lvol 1:The gain will recovery to the gain at the moment that the mode changes from AGC to Limiter.
4	RW	0x0	When the amplitude of the signal is more than 87.5% of the Full scale, use this signal to control the fast decrement(left channel): 0:Disabled 1:Enabled
3	RW	0x0	AGC noise gate function enable(left channel) 0:Disabled 1:Enabled
2:0	RW	0x1	AGC noise gate threshold(left channel) 000:-39dB 001:-45dB 010:-51dB 011:-57dB 100:-63dB 101:-69dB 110:-75dB 111:-81dB

Codec_REG51

Address: Operational Base + offset (0x00cc)

Codec register 51

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved

Bit	Attr	Reset Value	Description
5	RW	0x1	Left channel input PGA zero cross enable(left channel) 0:Update gain when gain register changes. 1:Update gain on 1st zero cross after gain register write.
4:0	RW	0x0c	Left channel input PGA gain(left channel) 00000:-18dB 00001:-16.5dB 00010:-15dB 01100:0dB 01101:+1.5dB 01110:+3dB 11111:+28.5dB

Codec_REG52

Address: Operational Base + offset (0x00d0)

Codec register 52

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Slow clock enabled(left channel) used for the zero cross timeout.
2:0	RW	0x0	Approximate sample rate(left channel) 000:48kHz 001:32kHz 010:24kHz 011:16kHz 100:12kHz 101: 8kHz 110~111:reserved

Codec_REG53

Address: Operational Base + offset (0x00d4)

Codec register 53

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x26	agc_max_l The low 8 bits of the AGC maximum level(left channel)

Codec_REG54

Address: Operational Base + offset (0x00d8)

Codec register 54

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x40	agc_max_h The high 8 bits of the AGC maximum level(left channel)

Codec_REG55

Address: Operational Base + offset (0x00dc)

Codec register 55

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x36	agc_min_l The low 8 bits of the AGC minimum level(left channel)

Codec_REG56

Address: Operational Base + offset (0x00e0)

Codec register 56

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x20	agc_min_h The high 8 bits of the AGC minimum level(left channel)

Codec_REG57

Address: Operational Base + offset (0x00e4)

Codec register 57

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	agcf AGC function select(left channel) 0: AGC function off 1: AGC function enable

Bit	Attr	Reset Value	Description
5:3	RW	0x7	pga_maxg Set maximum gain of PGA(left channel) 000:-13.5dB 001:- 7.5dB 010:- 1.5dB 011:+ 4.5dB 100:+10.5dB 101:+16.5dB 110:+22.5dB 111:+28.5dB
2:0	RW	0x0	pga_ming Set minimum gain of PGA(left channel) 000:-18dB 001:-12dB 010:- 6dB 011: 0dB 100:+ 6dB 101:+12dB 110:+18dB 111:+24dB

Codec_REG64

Address: Operational Base + offset (0x0100)

Codec register 64

Bit	Attr	Reset Value	Description
31:5	RO	0x0	reserved
4	RW	0x1	There are two methods to generate the control signals(right channel) 0: Normal way 1: Jack way

Bit	Attr	Reset Value	Description
3:0	RW	0x0	AGC hold time before gain is increased in normal mode.(right channel) 0000: 0ms 0001: 2ms 0010: 4ms 0011: 8ms 0100: 16ms 0101: 32ms 0110: 64ms 0111:128ms 1000:256ms 1001:512ms 1010: 1 s 1011~1111:0ms

Codec_REG65

Address: Operational Base + offset (0x0104)

Codec register 65

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:4	RW	0x2	Decay (gain ramp-up) time(right channel) Normal MODE(reg_agc_mde =0) 0000:500us 0001:1ms 0010:2ms 0011:4ms 0100:8ms 0101:16ms 0110:32ms 0111:64ms 1000:128ms 1001:256ms 1010:512ms 1001~1111:512ms

Bit	Attr	Reset Value	Description
3:0	RW	0x5	Attack (gain ramp-down) Time(right channel) Noraml MODE(reg_agc_mde =0) 0000:125us 0001:250us 0010:500us 0011:1ms 0100:2ms 0101:4ms 0110:8ms 0111:16ms 1000:32ms 1001:64ms 1010:128ms 1011~1111:125us Noraml MODE(reg_agc_mde =1) 0000:32us 0001:64us 0010:125us 0011:250us 0100:500us 0101:1ms 0110:2ms 0111:4ms 1000:8ms 1001:16ms 1010:32ms 1011~1111:32us

Codec_REG66

Address: Operational Base + offset (0x0108)

Codec register 66

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7	RW	0x0	Determines the AGC mode of operation(right channel) 0:AGC mode(normal mode) 1:Limiter mode
6	RW	0x1	AGC users zero cross enable(right channel) 0:Disabled 1:Enabled, the AGC gain will update at zero cross enable

Bit	Attr	Reset Value	Description
5	RW	0x0	When in the limiter mode, the low amplitude signal will recovery in two modes(right channel): 0:The gain will recovery to the value of the reg_pga_lvol 1:The gain will recovery to the gain at the moment that the mode changes from AGC to Limiter.
4	RW	0x0	When the amplitude of the signal is more than 87.5% of the Full scale, use this signal to control the fast decrement(right channel): 0:Disabled 1:Enabled
3	RW	0x0	AGC noise gate function enable(right channel) 0:Disabled 1:Enabled
2:0	RW	0x1	AGC noise gate threshold(right channel) 000:-39dB 001:-45dB 010:-51dB 011:-57dB 100:-63dB 101:-69dB 110:-75dB 111:-81dB

Codec_REG67

Address: Operational Base + offset (0x010c)

Codec register 67

Bit	Attr	Reset Value	Description
31:6	RO	0x0	reserved
5	RW	0x1	Left channel input PGA zero cross enable(right channel) 0:Update gain when gain register changes. 1:Update gain on 1st zero cross after gain register write.

Bit	Attr	Reset Value	Description
4:0	RW	0x0c	Left channel input PGA gain(right channel) 00000:-18dB 00001:-16.5dB 00010:-15dB 01100:0dB 01101:+1.5dB 01110:+3dB 11111:+28.5dB

Codec_REG68

Address: Operational Base + offset (0x0110)

Codec register 68

Bit	Attr	Reset Value	Description
31:4	RO	0x0	reserved
3	RW	0x0	Slow clock enabled(right channel) used for the zero cross timeout.
2:0	RW	0x0	Approximate sample rate(right channel) 000:48kHz 001:32kHz 010:24kHz 011:16kHz 100:12kHz 101: 8kHz 110~111:reserved

Codec_REG69

Address: Operational Base + offset (0x0114)

Codec register 69

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x26	agc_max_l The low 8 bits of the AGC maximum level(right channel)

Codec_REG70

Address: Operational Base + offset (0x0118)

Codec register 70

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved

Bit	Attr	Reset Value	Description
7:0	RW	0x40	agc_max_h The high 8 bits of the AGC maximum level(right channel)

Codec_REG71

Address: Operational Base + offset (0x011c)

Codec register 71

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x36	agc_min_l The low 8 bits of the AGC minimum level(right channel)

Codec_REG72

Address: Operational Base + offset (0x0120)

Codec register 72

Bit	Attr	Reset Value	Description
31:8	RO	0x0	reserved
7:0	RW	0x20	agc_min_h The high 8 bits of the AGC minimum level(right channel)

Codec_REG73

Address: Operational Base + offset (0x0124)

Codec register 73

Bit	Attr	Reset Value	Description
31:7	RO	0x0	reserved
6	RW	0x0	agcf AGC function select(right channel) 0: AGC function off 1: AGC function enable
5:3	RW	0x7	pga_maxg Set maximum gain of PGA(right channel) 000:-13.5dB 001:- 7.5dB 010:- 1.5dB 011:+ 4.5dB 100:+10.5dB 101:+16.5dB 110:+22.5dB 111:+28.5dB

Bit	Attr	Reset Value	Description
2:0	RW	0x0	pga_ming Set minimum gain of PGA(right channel) 000:-18dB 001:-12dB 010:- 6dB 011: 0dB 100:+ 6dB 101:+12dB 110:+18dB 111:+24dB

12.6 I2S Timing Diagram

12.6.1 Master mode

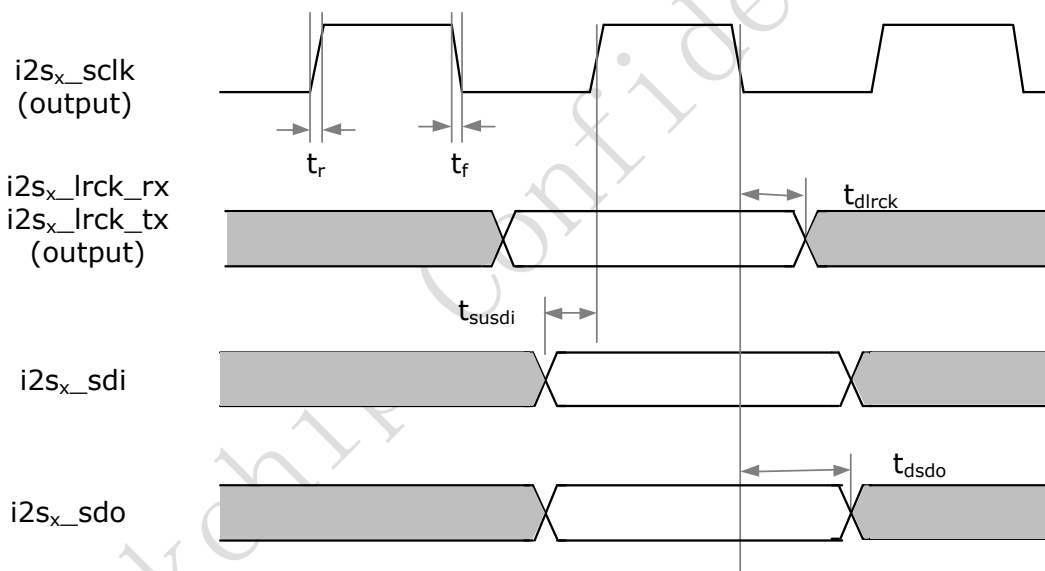


Fig. 12-15 Master mode timing diagram

Table 12-2 Meaning of the parameter in Fig. 9-1

*timing condition: VCCIO=3.3V, C_{LOAD}≤8pF, drive strength 4mA

Parameter	Min.	Typ.	Max.	Unit
t _r	i2s_x_sclk(output) rising time	-	-	39.84 ns
t _f	i2s_x_sclk(output) falling time	-	-	39.84 ns
t _{dlrck}	i2s_x_lrck_rx/i2s_x_lrck_tx propagation delay from i2s_x_sclk falling edge	3.96		ns
t _{susdi}	i2s_x_sdo setup time to i2s_x_sclk rising edge	4.86		ns
t _{dsdo}	i2s_x_sdi propagation delay from i2s_x_sclk falling edge	3.91	1.2	ns

12.6.2 Slave mode

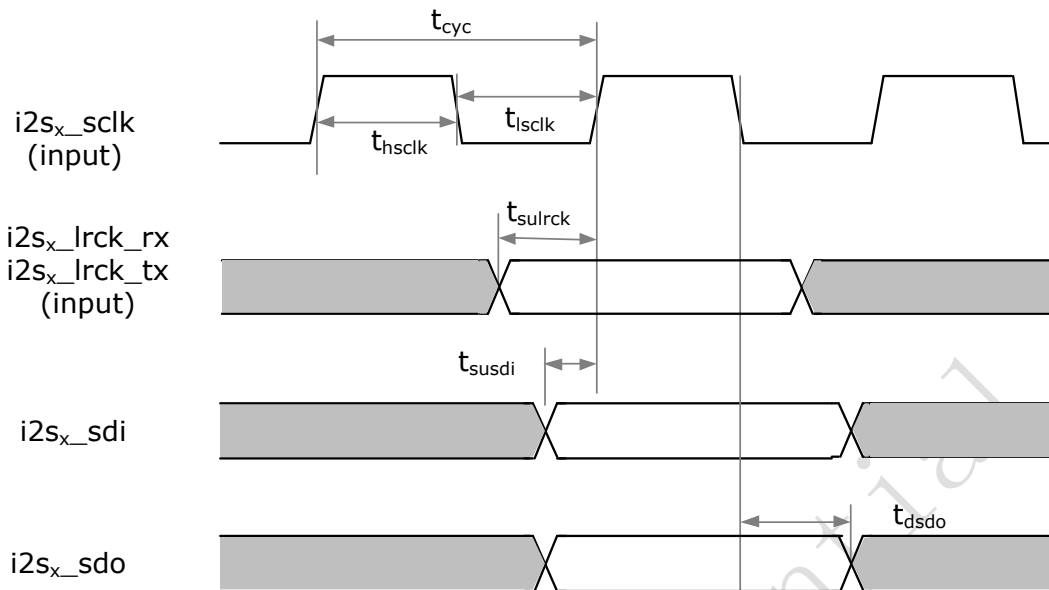


Fig. 12-16 Slave mode timing diagram

Table 12-3 Meaning of the parameter in Fig. 9-2

*timing condition: VCCIO=3.3V, C_{LOAD}≤8pF, drive strength 4mA

Parameter		Min.	Typ.	Max.	Unit
t _{cyc}	i2s_x_sclk cycle time	-	-	20	ns
t _{hclk}	i2s_x_sclk pulse width high	-	-	10	ns
t _{lclk}	i2s_x_sclk pulse width low	-	-	10	ns
t _{sulrck}	i2s_x_lrck_rx/i2s_x_lrck_tx setup time to i2s_x_sclk rising edge	3.94	-	-	ns
t _{susdi}	i2s_x_sdo setup time to i2s_x_sclk rising edge	2.06	-	-	ns
t _{dsdo}	i2s_x_sdi propagation delay from i2s_x_sclk falling edge	5.2	-	11.0	ns

12.7 Application Notes

It is recommended to enable DAC or ADC path according to the following flow sample. Just ADCL/DACL path showed below, and they have the same flow as ADCR/DACR with some detail register bit difference only.

1.enable BST_L to ADCL path

- (1)write 0x3f at offset address 0xac and write 0xff at offset address 0xb0.(hidden register,no register description)
- (2)write 0x3c to REG15 to set the reference current of ADC channel
- (3)write 0x24 to REG15 to set the reference voltage of ADCL channel
- (4)write 0x59 to REG16 to start BST_L
- (5)write 0x0e to REG 18 to start MININ_L, select muted BST_L connect to MIXIN_L .
- (6)write REG19 to set gain value of MIXIN_L.

- (7)write 0x4c to REG24 to start muted PGA_L, and set PGA_L to 0dB.
- (8)write 0x16 to REG42 to start ADCL clock module
- (9)write 0x06 to REG42 to start ADCL module
- (10)write 0x49 to REG16 to stop BST_L mute
- (11)write 0x06 to REG18 to stop MIXIN_L mute
- (12)write 0x0c to REG24 to stop PGA_L mute

2.enable DACL to SPKOUTL path

- (1)write 0x3f at offset address 0xac and write 0xff at offset address 0xb0.(hidden register,no register description)
- (2)write 0xbf to REG26 to set reference current of DAC channel
- (3)write 0x8e to REG26 to set reference voltage of DACL channel
- (4)write 0x1e to REG27 to set DACL clock module
- (5)write 0x16 to REG27 to start DACL module
- (6)write 0x1c to REG 29 to start HPMIXL and initialize HPMIXL
- (7)write 0x60 to REG35 to start SPKOUTL and initialize gain value to -39 db for muted SPKOUTL
- (8)write 0x20 to REG35 to stop initialization of SPKOUTL.
- (9)write 0xef to REG30 to connect DACL with HPMIXL
- (10)write 0x36 to REG27 to stop initialization of DACL.
- (11)write 0x0c to REG29 to stop initialization of HPMIXL.

3.enable MICBIAS

- (1)write 0x3c to REG15 to set reference current of ADC channel
- (2)write REG39 to set related parameters.

4.AGC

- (1)write REG52 to set audio sample rate.
- (2)write REG53/54/55/56 to set AGC level.
- (3)write REG50 to set AGC mode
- (4)write REG57 to enable AGC, it's recommend to write 0x78.
- (5)write REG10 to select left or right channel ACG output to control PGA gain.

Chapter 13 display path

13.1 Overview

There are two kinds for display path, "same source to dual panel" and "different sources to dual panel".

13.2 Application Notes

There are 5 signals in CRU to configure out different display path (cfg_vif0_bypass, cfg_vif1_bypass, cfg_scalerin_sel, cfg_dither_sel and cfg_hdmi_sel). And there are 4 signals to control VIF0, VIF1, SCALER and DITHER (vif0_en, vif1_en, scl_en, frc_dither_en).

There are two groups LCDDC input IO (LCDDC0 and LCDDC1). And LCDDC1 can also be set as output IO after DITHER, then frc_dclk_inv should be set "1". There is another LCDDC output IO group (reused with LVDS IO), then LVDS should be set as ttl mode.

Here is display path configuration table for reference.

Table 133-1 display path configuration

same source to dual panel	L C D C O	S D R	LCDDC0+HDMI; LCDDC0+DITHER; -->LCD1(IO output)	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDDC1 IOMUX as output frc_dclk_inv=1;
	L C D C O	S D R	LCDDC0+HDMI; LCDDC0+SCALER+DITHER ; -->LCD1(IO output)	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=0; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=2; LCDDC1 IOMUX as output frc_dclk_inv=1;

	L C D C O	S D R / D D R	VIF0+HDMI; VIF0+DITHER; -->LCD1(IO output)	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDC1 IOMUX as output frc_dclk_inv=1;
	L C D C O	S D R / D D R	VIF0+HDMI; VIF0+SCALER+DITHER; -->LCD1(IO output)	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=0; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=2; LCDC1 IOMUX as output frc_dclk_inv=1;
	L C D C O	S D R / D D R	VIF0+HDMI; VIF0+SCALER+DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=0; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C O	S D R / D D R	VIF0+HDMI; VIF0+DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;

	L C D C 0	S D D R	HDMI; DITHER;-->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C 0	S D R / D D R	VIF0+DITHER;-->MIPI/L VDS VIF0+SCALER+HDMI; LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=0; scl_en=1; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C 0	S D R / D D R	VIF0+DITHER;-->MIPI/L VDS VIF0+HDMI; LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C 0	S D D R	DITHER;-->MIPI/LVDS SCALER+HDMI; LCD1 input;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=0; scl_en=1; cfg_dither_sel=0; cfg_hdmi_sel=1; LCDC1 IOMUX as input frc_dclk_inv=0;

	L C D C 0	S D D R	DITHER;-->MIPI/LVDS HDMI; LCD1 input	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C 1	S D R / D D R	VIF1+HDMI; VIF1+SCALER+DITHER;- ->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=0; vif1_en=1; cfg_scalerin_sel=1; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C 1	S D R	HDMI; SCALER+DITHER;-->MIPI /LVDS LCD1 input;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=1; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;
	L C D C 1		Not support LCDC1->DITHER; Only support LCDC1->SCALER->DITHE R	
different sources to dual panel	L C D C 0	S D R / D D R	VIF0+SCALER+DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=0; vif1_en=1; cfg_scalerin_sel=0; scl_en=1; cfg_dither_sel=0;

L C D C 1	S D R / D D R	VIF1+HDMI;	cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 0	S D R / D D R	VIF0+DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0;
L C D C 1	S D R / D D R	VIF1+HDMI;	cfg_dither_sel=0; cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 0	S D R / D D R	VIF0+DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=0;
L C D C 1	S D R	HDMI;	cfg_dither_sel=0; cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 0	S D R	DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=0; vif1_en=1; cfg_scalerin_sel=X;
L C D C 1	S D R / D D	VIF1+HDMI;	scl_en=0; cfg_dither_sel=0; cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;

	R		
L C D C 0	S D R	DITHER; -->MIPI/LVDS LCD1 input;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=X; scl_en=1;
L C D C 1	D D R	HDMI;	cfg_dither_sel=0; cfg_hdmi_sel=0; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 0	S D / D D R	VIF0+HDMI;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=0; vif1_en=1; cfg_scalerin_sel=1;
L C D C 1	S D / D D R	VIF1+SCALER+DITHER; -->MIPI/LVDS LCD1 input;	scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 0	S D / D D R	VIF0+HDMI;	cfg_vif0_bypass=0; vif0_en=1; cfg_vif1_bypass=0; vif1_en=1; cfg_scalerin_sel=1; scl_en=1;
L C D C 1	S D R	SCALER+DITHER; -->MIPI/LVDS LCD1 input;	cfg_dither_sel=1; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C	S D R	HDMI;	cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0;

	0			cfg_scalerin_sel=1; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 1	S D R / D D R	VIF1+SCALER+DITHER; -->MIPI/LVDS LCD1 input;		
L C D C 0	S D D R	HDMI;		cfg_vif0_bypass=1; vif0_en=0; cfg_vif1_bypass=1; vif1_en=0; cfg_scalerin_sel=1; scl_en=1; cfg_dither_sel=1; cfg_hdmi_sel=2; LCDC1 IOMUX as input frc_dclk_inv=0;
L C D C 1	S D D R	SCALER+DITHER; -->MIPI/LVDS LCD1 input;		

Note: The datapath to hdmi, which don't like others, it has two cfg register, one is for clock path(cfg_misc_con[13:12]), one is for data path(cru_clkssel3_con[13:12]). And the datapath from scaler to hdmi is disable.

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